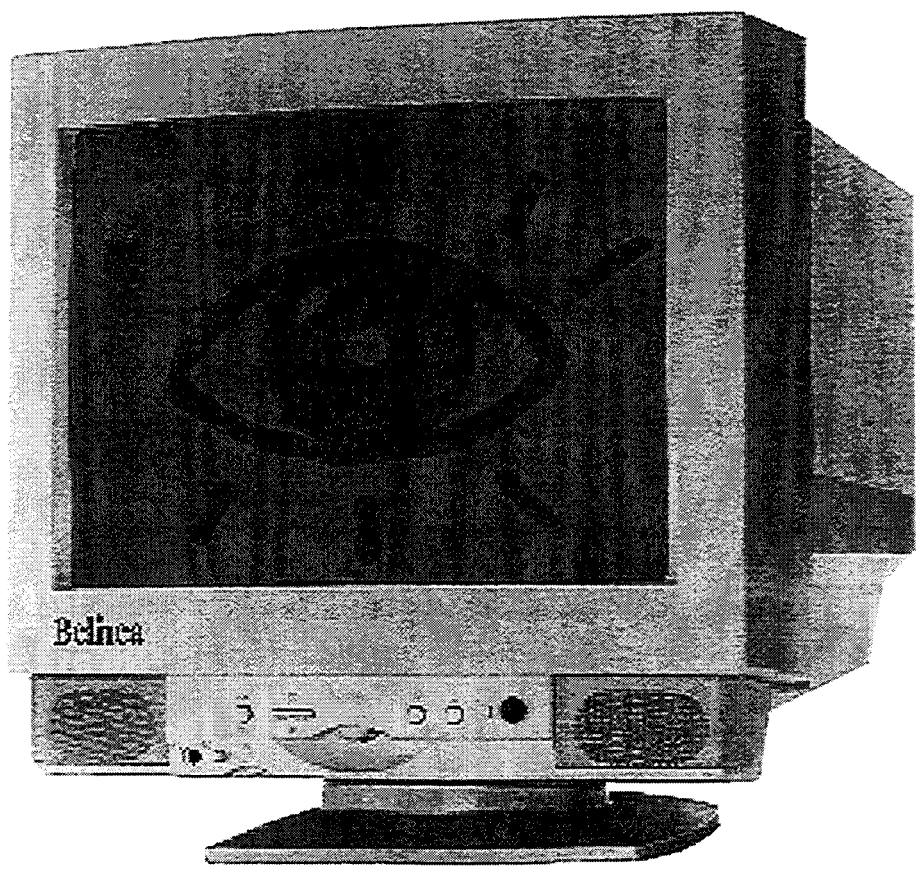
Belinea 10 55 96

Color Monitor
Service Manual



BELINEA
10 55 96

Service Manual

BELINEA
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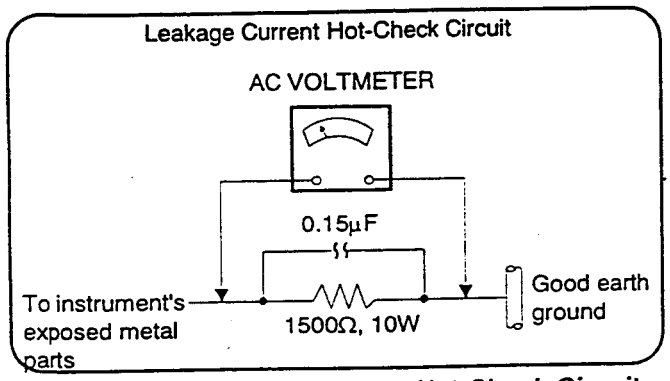
Service Manual

Leakage Current Hot Check

1. Plug the AC cord into the AC outlet. Do not use an isolation transformer for this check.
2. Connect a 1.5k, 10 watt resistor in parallel with a 0.15F capacitor between each exposed metallic part on the set and a good earth ground (see How to Find a Good Earth, below) as shown in the diagram below.



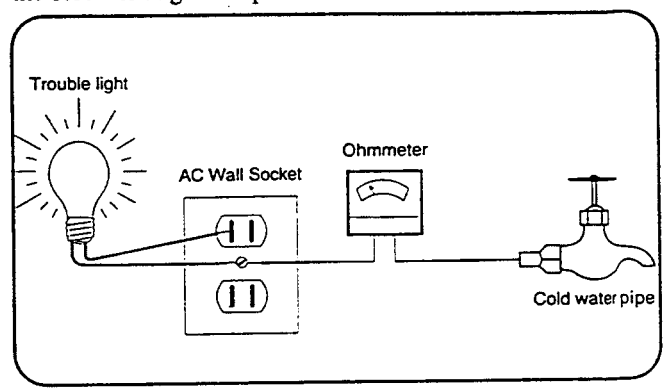
Example of Leakage Current Hot-Check Circuit

3. Use an AC voltmeter with 1000 ohms/volt or more sensitivity to measure the potential across the resistor.
4. Check each exposed metallic part, and measure the voltage at each point.
5. Reverse the polarity of the AC plug in the AC outlet and repeat the above measurements.
6. The potential at any point should not exceed 0.75 volt RMS. A leakage current tester (Simpson Model 229, RCA WT-540A or equivalent) may be used to make the hot checks.

Leakage current must not exceed 0.5 milliamp. If a measurement is outside of the specified limit, there is a possibility of a shock hazard and the monitor should be repaired and rechecked before it is returned to the customer.

How to Find A Good Earth

A cold water pipe is a guaranteed earth ground; the cover plate retaining screw on most AC outlet boxes is also at earth ground. If the retaining screw is to be used as your earth ground, verify that it is at ground by measuring the resistance between it and a cold water pipe with an ohmmeter. The reading should be zero (0) ohms. If a cold water pipe is not accessible, connect a 60-100 watt trouble light (not a neon lamp) between the hot side of an AC power receptacle and the retaining screw. Try both slots, if necessary, to locate the hot side of the line. The lamp should light at normal brilliance if the screw is at ground potential



How to Check for Earth Ground

Preface
Before You Start

General Safety Precautions

1. Use an isolation transformer in the power line and AC supply to troubleshoot.
2. When servicing, observe the original lead dress, especially in the high voltage circuits. If a short circuit is found, replace all parts which have been overheated or damaged.
3. Before turing the display on, measure the resistance between B+ line and chassis ground. Connect the negative side of an ohmmeter to the B+ lines and the positive side to chassis ground. Each line should have more resisstance than the following specifications:

B+ Line	Minimum Resistance
+200V	134.5KΩ
+77V	60.51KΩ
+15.0V	30.54KΩ
+12.0V	12.63KΩ
+15V	27.13KΩ
+6.3V	4.150Ω
+5.0V	20.62KΩ

4. Potentials, as high as 25kV are present when this display is in operation. Operation of the display without the rear cover involves the danger of a shock hazard from the display power supply. Servicing should not be attempted by anyone who is not thoroughly familiar with the precautions necessary when working on high voltage equipment. Always discharge the anode of the picture tube to the display chassis before handling the tube.
5. After servicing, be sure to check the items listed in the Safety Checkout, below before returning the serviced unit to the customer.

Safety Checkout

The following checks must be made after correcting the original service problem and before the unit is returned to the customer.

1. Check the area of your repair for unsoldered or poorly soldered connections. Check the entire board surface for solder splashes and bridges.
2. Check the inter board wiring to ensure that no wires are pinched or coated with high-wattage resistors.
3. Check that all control knobs, shields, covers, ground straps and mounting hardware have been replaced. Makde absolutely sure you have replaced all the insulators.
4. Look for any unauthorized replacement parts, particularly transistors, that may have been installed dueing a previous repair. Point them out to the cusstomer land recommend their replacement.
5. Look for parts which, though functioning, show obvious signs of deterioration. Point them out to the customer and recommend their replacement.
6. Check the line cord for cracks and abrasion. Recommend the replacement of any such line cord to the customer.
7. After making any repair, check the B+ and HV to see whether they are at the values specified. Make sure your instruments are accurate; if your HV meter always shows a low HV, check the meter to ensure it is not malfunctioning.
8. Carry out the leakage current checks as detailed below overleaf.

Leakage Current Cold Check

1. Unplug the AC cord and connect a jumper between the two prongs on the plug.
2. Turn on the display power switch.
3. Use an ohmmeter to measure the resistance value between the jumpered AC plug and each exposed metallic cabint part on the display, such as screwheads, terminals control shafts, etc. When an exposed metallic part has a return path to the chassis, the reading should be between 240k and 5.2M. When exposed metal does not have a return path to the chassis, the reading must be.

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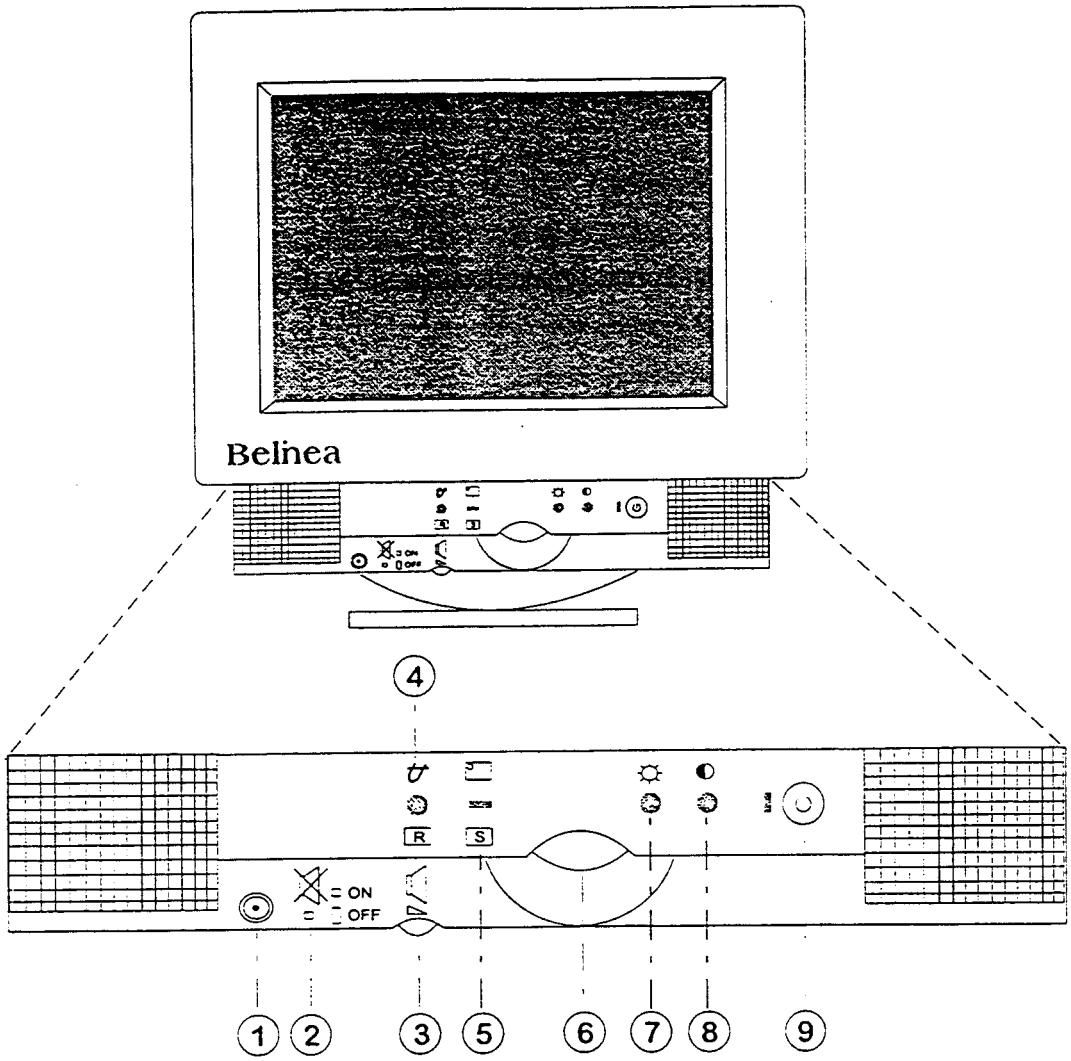
1.1. Monitor Control Locations & Functions



KEY TO BUILT-IN MONITOR CONTROL FUNCTIONS		
(1)	Head Phone Jack	This jack is used to connect a head phone.
(2)	Mute Key	Use mute button, when active shall mute the internal speakers and external earphone.
(3)	Audio Volume VRs	Used to control audio volume.
(4)	Manual Degauss and Factory Setting Recall Function	Digital control for manual degauss of monitor at the normal condition and for recall the origional factory setting, during OSD pattern is on screen.
(5)	Push Button for OSD ON/OFF and Thumbwheel Enter Confirm	Press to call up OSD function into screen and confirm the thumbwheel enter for icon.
(6)	Thumbwheel for Adjusting Setting and OSD Function Selection	Thumbbwheel for adjusting the setting, clockwise for increasing and counterclockwise for decreasing and selection the OSD function icon.
(7)	Brightness Control Button	Increase / decrease raster black level using thumbwheel adjusting, clockwise for increasing and counterclockwise for decreasing.
(8)	Contrast Control Button	Increase / decrease video gain using thumbwheel adjusting, clockwise for increasing and counterclockwise for decreasing.
(9)	Power On/Off	Hard power On/Off button. Adjacent LED is lit when on. The LED color is green for normal condition and change to orange for DPMS condition.

1.2. Product Overview

The monitor installed in the Belinea 10 55 96 (RTS 7K25/6) phom described in this service manual has the following features:

- ☐ 17 inches 0.26 dot pitch conventional CRT
- ☐ 30-85 kHz horizontal scanning
- ☐ 50Hz~120Hz vertical refresh rate scanning
- ☐ 28 total memory modes in standard configuration
- ☐ Universal segmented auto range power supply
- ☐ VESA/NUTEK/EPA compliant power management

1.3. CRT Characteristics

- ☐ Screen Size..... 17 inches
- ☐ Faceplate Type..... Fs
- ☐ Orientation..... Landscape
- ☐ Phosphor Dot Pitch ..... 0.26mm, delta arrangement
- ☐ Electron Gun 29mm,Precision-In-Lin
- ☐ Deflection Angle ..... 90 degree diagonal
- ☐ Shadow Mask..... Invar
- ☐ Phosphor Type..... P22
- ☐ Phosphor Persistence.... Medium Short
- ☐ Faceplate Properties..... ASN coating,anti-static, anti-reflection
- ☐ Standard Light Transmission 53.5% Typical

1.4. Power Specifications

1.4.1. Power Supply

- ☐ A/C Receptacle IEC320
- ☐ Power Supply Type ..... Universal
- ☐ A/C Line Voltage Ranges 88VAC-132VAC 180VAC-264VAC
- ☐ A/C Line Frequency Ranges 50Hz/60Hz±3Hz
- ☐ Inrush Current ..... 30A/132V or 50A/264V(at cold start)
- ☐ Leakage Current..... ≤3.5mA
- ☐ Degauss ..... Automatic and Manual (20 minutes for a full recovery)

1.4.2. Power Management

☐ Summary of operating states:

APM State	LED Color	Power Consumption	Automatic Recovery Time
on	green	<150W	not applicable
standby	orange	<30W	<3 seconds
suspend	orange	<8W	<10 seconds
off	orange	<8W	<10 seconds
self test	green	<150W	not applicable

- ☐ Signaling compliant with VESA DPMS guidelines
- ☐ Nutek 1992 guidelines suspend < 30 watts; off < 8 watts
- ☐ EPA energy star standby < 30 watts

1.5. Integrated Audio Specifications

1.5.1. Audio Power Amplifier

- ☐ Output power..... 1.5W per channel minimum, @ 10% THD at 1kHz
- ☐ Supply Voltage ..... +12VDC, 0.5V, 30mA-0.6A (average 0.25A)
- ☐ Frequency response..... 100Hz to 15kHz, 3dB
- ☐ Input level ..... 1V rms

1.5.2. Speakers

- ☐ Speaker type ..... 40mmx70mm oval cone typex2
- ☐ Impedance ..... 8 ohms @ 800Hz
- ☐ Rated input power..... 2 W
- ☐ Frequency response..... Up to 15kHz, 20dB maximum

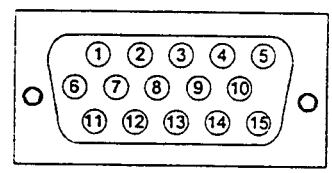
1.6. Video Specifications

1.6.1. Video Amplifier Performance

- ☐ Bandwidth (dot rate).... 135MHz
- ☐ Typical 10%~90% rise and fall times...calculation 5.5ns
- ☐ Video generator rise/fall times...2ns maximum
- ☐ Scope and probe bandwidth.....350MHz minimum
- ☐ Probe capacitance 2.5Pf
- ☐ Overshoot/Undershoot .. 10% maximum
- ☐ Sync on green ..... Amplitude:714mV maximum Sync on Green Amplitude:286mV maximum

1.6.2. Video Input Signal Characteristics

- ☐ Video Type ..... Analog
- ☐ Amplitude ..... 700mV maximum
- ☐ Video Input Impedance.. 75 Ohms±1%
- ☐ Optional DD 1/2B Video Connector Pin Assignments:



pin	Signal	pin	Signal
1	Red video	9	No pin
2	Green video	10	Sync return
3	Blue video	11	Monitor GND
4	Monitor GND	12	SDA(bi-directional)
5	No pin	13	H. sync
6	Red return	14	V. sync (VCLK)
7	Green return	15	SCL
8	Blue return		

1.7. Sync Input Signal Characteristics

1.7.1. Separate Sync

- ☐ Sync Type ..... TTL
- ☐ Amplitude ..... 2.4V minimum(Logic High)
  0.8V max.(Logic Low)
- ☐ Polarity ..... Positive or Negative
- ☐ Equalization pulses ..... Not allowed

1.7.2. Composite Sync

- ☐ Sync Type ..... TTL
- ☐ Amplitude ..... 2.4V minimum(Logic High)
  0.8V max.(Logic Low)
- ☐ Polarity ..... Positive or Negative
- ☐ Serration pulses ..... Allowed at horizontal rate
- ☐ Equalization pulses ..... Not allowed

1.7.3. Sync On Green

- ☐ Sync Type ..... As per Apple
- ☐ Amplitude ..... 0V min(Logic High)
  -286mV max.(Logic Low)
- ☐ Polarity ..... Negative/Composite
- ☐ Serration pulses ..... Allowed at horizontal rate
- ☐ Equalization pulses ..... Not allowed

1.8. Environmental

1.8.1. Temperature/Humidity/Altitude

OPERATING

- ☐ Temperature..... 10°C to 35°C
- ☐ Relative Humidity 0 to 90%,non-condensation
- ☐ Altitude ..... 0 to 10,000 feet

NON-OPERATING

- ☐ Temperature..... -40°C to +65°C
- ☐ Relative Humidity..0 to 95%,non-condensation
- ☐ Altitude ..... 0 to 40,000 feet

1.8.2. Vibration Test

UNPACKED UNIT

Operating without package:

	Frequency	Amplitude	Acceleration(G)
1	5-22Hz	0.25mm	-
2	22-500Hz	-	0.25G

Times/Cycle:

- ☐ Rise Time..... 10 Minutes
- ☐ Fall Time ..... 10 Minutes
- ☐ Number of Sweeps ..... 1 Cycle
- ☐ Axis..... X,Y,Z
- ☐ Total Times..... 60 Minutes

PACKAGED UNIT

Storage with package:

	Frequency	Amplitude	Acceleration(G)
1	5-50Hz	-	0.83G
2	-	-	-

Times/Cycle:

- ☐ Rise Time ..... 10 Minutes
- ☐ Fall Time..... 10 Minutes
- ☐ Number of Sweeps ..... 1 Cycle
- ☐ Axis..... X,Y,Z
- ☐ Total Times..... 60 Minutes

1.8.3. Drop Test

- ☐ Compliant with NSTA Project 1A guidelines
- ☐ Drop Height 46cm
- ☐ Test Direction ..... 1 Corner, 3 Edges, 6 Faces

1.9. Preset Timing Modes

This display has 10 preset display modes configured during manufacture, given in the following table.

Notes: Custom Require: from lot #5 change preset timing modes is the table A to table B.

Table A:

Model No.	Hf KHz	Vf Hz	Dot x Line
01	63.980	60.010	1280x1024
02	56.476	70.070	1024x768
03	48.363	60.004	1024x768
04	46.875	75.000	800x600
05	37.861	72.809	640x480
06	37.500	75.000	640x480
07	35.156	56.250	800x600
08	31.469	59.942	640x480
09	31.469	70.080	640x400
10	31.469	70.080	640x350

Table B:

Model No.	Hf KHz	Vf Hz	Dot x Line
01	79.976	75.025	1280x1024
02	68.677	84.997	1024x768
03	61.080	75.782	1024x768
04	60.023	75.029	1024x768
05	53.674	85.061	800x600
06	46.875	75.000	800x600
07	43.269	85.008	640x480
08	37.500	75.000	640x480
09	31.469	59.942	640x480
10	31.469	70.080	640x400

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2.1. Removing the Rear Cover

1. Remove the four screws at the rear of the display. Refer to the figure 2-1 (A).
2. Remove the rear cover.

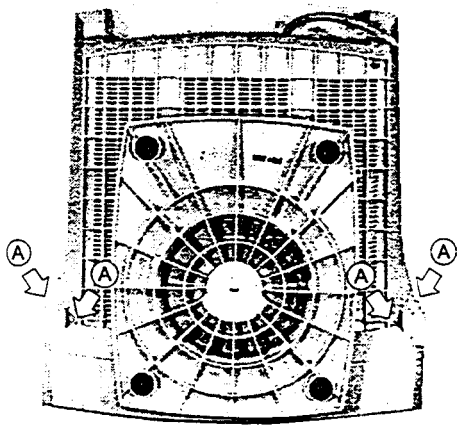

Figure 2-1 Remove the Rear Cover

2.2. Remove Top Shield and Rear Shield

1. Disconnect the three ground wires. Refer to the figure 2-2 (A).
2. Remove the three screws at the top shield. Refer to the figure 2-2 (B).
3. Disconnect the two ground wires. Refer to the figure 2-3 (A).
4. Remove the three screws at the top shield. Refer to the figure 2-3 (B).
5. Release the cord cramp. Refer to the figure 2-3 (C).
6. Remove top shield and rear shield.

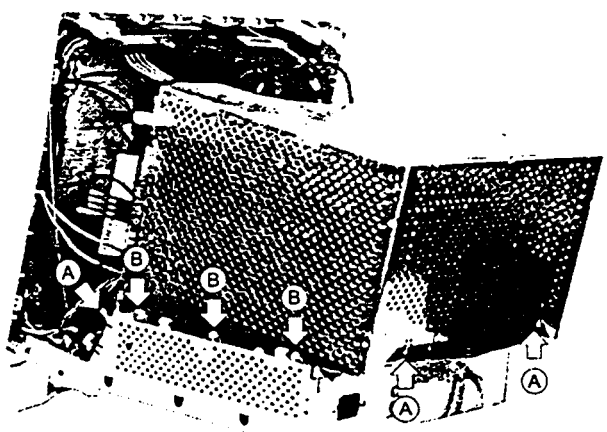

Figure 2-2 Remove the Top Shield & Rear Shield

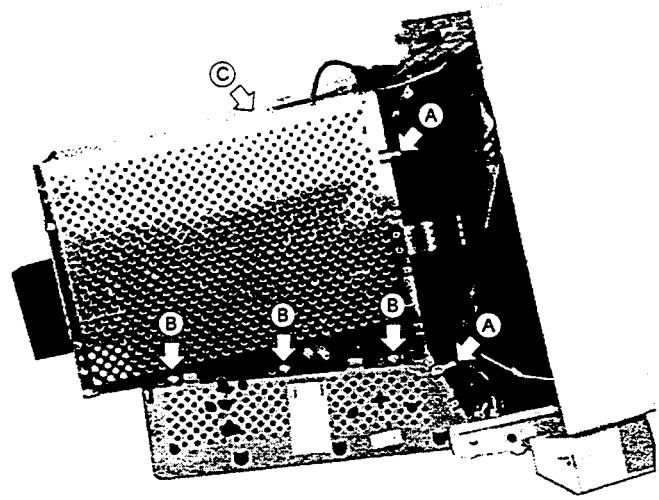

Figure 2-3 Remove the Top Shield & Rear Shield

2.3. Internal Disassembly (Right Side)

The neck board is plugged on to the CRT neck and is enclosed in a metal shielding.

1. Disconnect the two ground wires. Refer to the figure 2-4 (A).
2. Remove the two connected pins from the main board. Refer to the figure 2-4 (B).
3. Remove the screw at the bezel. Refer to the figure 2-4 (C).
4. Remove the nylon revets holding from bezel. Refer to the figure 2-4 (D).

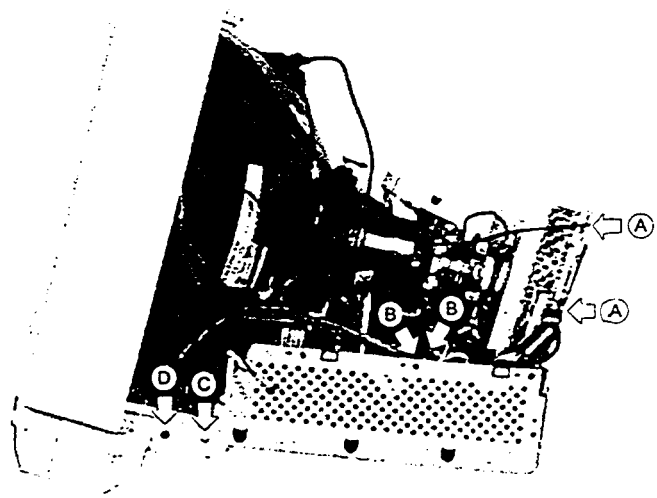

Figure 2-4 Internal Disassembly (Right Side)

2.4. Internal Disassembly (Left Side)

1. Disconnect the ground wire. Refer to the figure 2-5 (A).
2. Remove the connected pin. Refer to the figure 2-5 (B).
3. Remove the two connected pins from the main board. Refer to the figure 2-5 (C).
4. Remove the connected pin from neck board. Refer to the figure 2-5 (D).

IMPORTANT NOTE

To avoid risk of electric shock, before removing the anode cap, made sure tdhe anode has been completely discharged as high voltage may remain on the anode for extended time after power off.

5. Remove the anode cap from the CRT. Refer to the figure 2-5 (E).
6. Remove the screw at the bezel. Refer to the figure 2-5 (F).
7. Remove the nylon revets holding from bezel. Refer to the figure 2-5 (G).

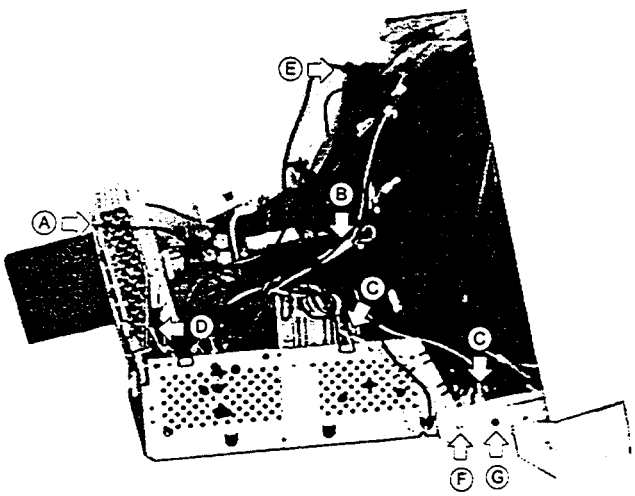

Figure 2-5 Internal Disassembly (Left Side)

2.5. Removing the Neck Board & Main Board

1. Disconnect the three ground wires from the neck shield. Refer to the figure 2-6 (A).
2. Remove the neck shield.
3. Remove the neck board.
4. Remove the main board.

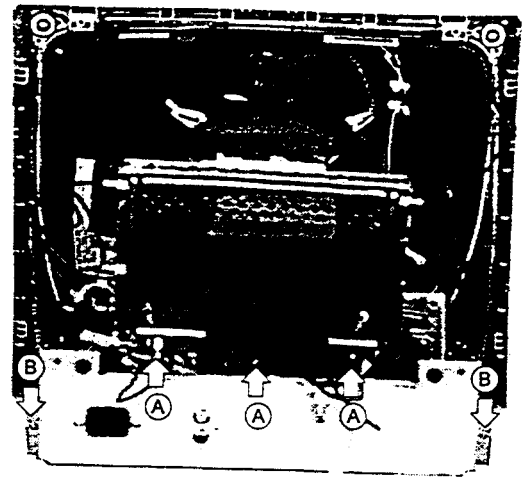

Figure 2-6 Remove Neck Board & Main Board

2.6. Remove the Control Board

1. Remove the two screws from the control panel. Refer to the figure 2-6 (B).
2. Remove the control panel.
3. Remove the three screws from the control board. Refer to the figure 2-7 (A).
4. Remove the Control Board.
5. Remove the screw from control panel. Refer to the figure 2-7 (B).
6. Remove the earphone board.

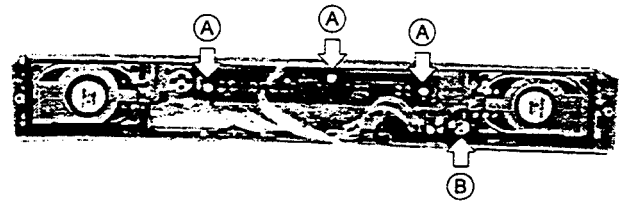

Figure 2-7 Remove the Control Board and Earphone Boaed

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3.5. Audio Amplifier 3-14

3.1. Switching Power Supply

The switching power supply (SPS) used in this display is a 150W flyback mode type. The power supply provides seven outputs (B+, 77V, 15V, -15V, 6.3V ,+15V and +5V). Please refer to schematic diagram for details of the circuit layout. The input voltage is from 88VAC — 264VAC with an input frequency of 47Hz — 63Hz. as shown in figure 3-1.

The current first passes through the EMI control circuit and is regulated to DC by the bridge diodes (BD901) and filter capacitor (C907). During rectification a large current surge is generated and as C907 has a very low impedance while being charged the fuse, on/off switch and bridge diode are all liable to be damaged. For this reason, a thermal resistor (NTCR) is added before the bridge diode in order to limit the large current surge generated during the charging of the capacitor.

During rectification, C910 is charged through R903 and R904. When C910 is charged to 16V, IC901 3842A starts to operate (for details, of the functions of this IC, please refer to the relevant data sheet) and outputs a pulse signal from Pin 6 to set the transistor Q902 in the ON state. At this time, transformer T903, which is connected in parallel, starts to store power. When the current passing through the resistor R914, and the supplementary current from R957 and R964 into Pin 3 of IC901 reaches 1.1V, IC901 is reset, causing the energy stored by the transformer to reach the rated value. In order to prevent the transformer from being saturated and causing damage to the transistor, when transistor Q902 is in the OFF state, the energy stored in the transformer T903 is released into the secondary coil and is regulated through the various output loops and filters and converted to the required DC output. In addition to this, at the appropriate time, the windings pin1 — pin2 supply Pin 7 of IC901 with a fixed power supply for normal operation. Also, when windings pin2 — pin3 are in power saving active state, power is supplied to Pin 7 of IC901 for normal operation.

In any of the above cased, the output pulse is terminated and the FET is turned off, causing the voltage on the output of the FET to rise rapidly, and the voltage across the winding of the primary to reverse in polarity, thus tending to reset the flux within the core. At this point, the diodes D915, D925, D917-D920 and D926 on the secondary supply winding become forward biased and begin to conduct, thus transferring energy from primary to the secondary, and charging the secondary capacitors.

There is also secondary winding the primary side of the power supply which, through diode D908 and Q901 recharges the control IC901 reservoir capacitor C910. This supply then keeps the IC901 running. In the event of a secondary short circuit, the supply fails to recharge, thus the voltage across C910 drops to a threshold limit below which the IC901 cuts out and returns to its low current load operation.

During normal operation, the supply rails charge until the error amplifier realized by IC903 on the secondary begins to turn on the opto-coupler, PH901. At this point, the photo-transistor of this opto-coupler on the primary side begins to conduct, draining current from the primary control IC901 supply through diode D907 and D928.

Under normal operation IC903 regulates the current flow through PH901, and hence determines the output voltage of the error amplifier internal to IC901. Various passive components around IC903 and IC901 set the gain compensation for optimum stability and regulation characteristics.

In the event of a fault condition occurring, either Q904 may be turned on by the lack of voltage at pin2 of IC901 or zener diode ZD903 may conduct, due to excessive voltage on the primary IC901 supply. In the latter case, the triac Q903 will fire, thus dragging down the output of the control IC901 error amplifier, which in turn will limit the duty cycle and reduce the output voltage. It will stay in this mode until the AC input power is removed.

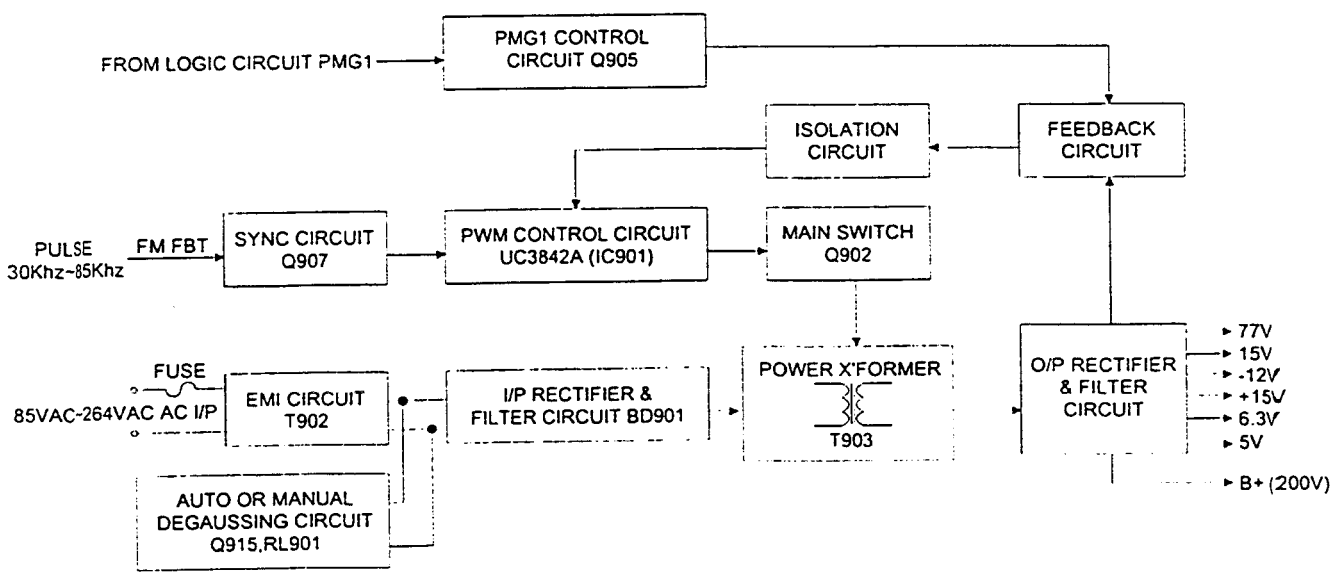


Figure 3-1 Switching Power Supply Block Diagram

When the feedback signal passing through the main 77V output is completed, the transistor's duty cycle is adjusted through the transfer to Pin 2 of IC901 3842A of the primary coil by PH901 4N35 and IC903 TL431, stabilizing the output current. At this time, it is important to note that before the feedback signal is established, the charge level of C917 cannot trigger Q903 SCR or it will cause a faulty power startup. In addition, in order to synchronize the supply power and monitor and reduce noise that will cause interference to the display, in the area D913 the monitor's feedback transformer gets a feedback signal in order to ensure synchronization between the power supply and monitor, with synchronization in the range 30kHz — 85kHz. Because the power operating frequency changes with the monitor causing changes in the value of IP, (the value of LP is fixed while the value of IP increase or decreases according to the frequency), this affects the test value of Pin 3 of IC901 3842A. This causes the total power supplied to vary according to the frequency, so a compensation value is provided by D914 in order to reduce the difference in total power for different frequencies. In addition, because the AC input ranges from 85VAC to 264VAC, this causes the value of the direct current on the DC bus to vary, affecting the rise rate of IP, the oscillator and the duty cycle, and causing the test value obtained at Pin 3 of IC901 to vary. To resolve this, a compensation value is provided by R964 and R957 which reduces the difference resulting from the different input voltages.

3.1.1. Auto-degaussing

When base of Q915 connector is in high state, the transistor Q915 2SC945P is on, causing the relay to jump from Normal Open (N.O.) to Normal Close (N. C.) to perform auto-degaussing operations. The duration of this operation is controlled by a logic pulse and lasts approximately 6 (six) seconds. When transistor Q915 enters the OFF state and the relay returns to N.O. to terminate the auto-degaussing operation is completed.

3.1.2. Suspend Mode Operation

Two feedback ratios can be selected, both sensing from the 78V rail. In the event of Q905 being turned on by micro processor, additional current is drawn from the virtual earth node of IC903, thus causing the power supply to serve the rail to a high voltage, nominally 78V. This is trimmed by resistor R937, R940 and R941. The other supply rail are predetermined ratios of this winging, being +15V,-12V,+6.3V and +200V nominally. In addition, a low voltage primary side winding feeds the control IC901 directly through D907 turning off the control IC901 supply through Q901, which would otherwise dissipate excessively.

When Q905 is turned off, the 78V rail drop to around 17V. In this case, the primary control supply fed through D907 drops to a value that is below the level needed to sustain operation. Instead, Q901 begins to conduct and the higher voltage supply winding taken via D908 is used to keep the primary side powered up with minimal power losses.

The 5V power supply is driven by one of two sources, In normal operation when the 78V is present, the 5V regulator, IC902 is fed from the 15V rail through diode D921. When switched to standby mode (78V rail drops to 12V) then the 15V rail drops too low to supply IC902. In this case Q906 take over and maintains the supply to IC902 at around 9V.

In addition to the 5V regulated supply, in normal operation there is also a 15V regulated supply take from the 15V rail.

To ensure that micro processor gets a good 5V power supply, there is a power good detection circuit formed by Q801 and Q802. This monitors the supply going into the 5V rail (not the 5V rail directly). It detects whether there is sufficient voltage to enable the 5V regulator to work effectively. It is not a detection of the 5V rail itself, but relies upon the premise that the regulator is not faulty and that there is no faulty load condition on the 5V.

During power up, there is a delay to the signal at the output of the threshold comparator Q801 and Q802 a caused by ZD801 and C801, in order to allow the micro circuit time to stabilize. The threshold is chosen such that the RESET line drops low at least 25ms before the 5V drop out of regulation.

Finally a synchronization pulse taken from the horizontal output stage maintains the SMPS operating frequency in sync with the horizontal scan. D913 injects a pulse which prematurely triggers the oscillator within IC901 which would otherwise run at a frequency lower than the minimum required sync frequency.

3.2. The Deflection Circuit

Please refer to the block diagram of the deflection circuit and video circuit and Logic circuit as shown in figure 3-2.

3.2.1. IC301 LM1291 Video PLL System for Continuous-Sync

The LM1291 is an integrated horizontal time base solution specifically designed to operate in continuous-sync video monitors. It automatically synchronizes to any H ferquency from 30kHz to 85kHz and provides the drive pulse to the high power deflection circuit.

Available sync processing includes a vertical sync separator and a composite video sync stripper. An internal sync selection scheme gives highest priority to separate H and V sync, then composite sync, and finally sync on video, no external switching between sync sources is necessary is necessary. The LM1291 provides polarity-normalized H/HV and V sync outputs, along with logic flags which show the respective input polarities.

The design uses an on-chip FVC (Frequency to Voltage Converter) to set the center frequency of the VCO

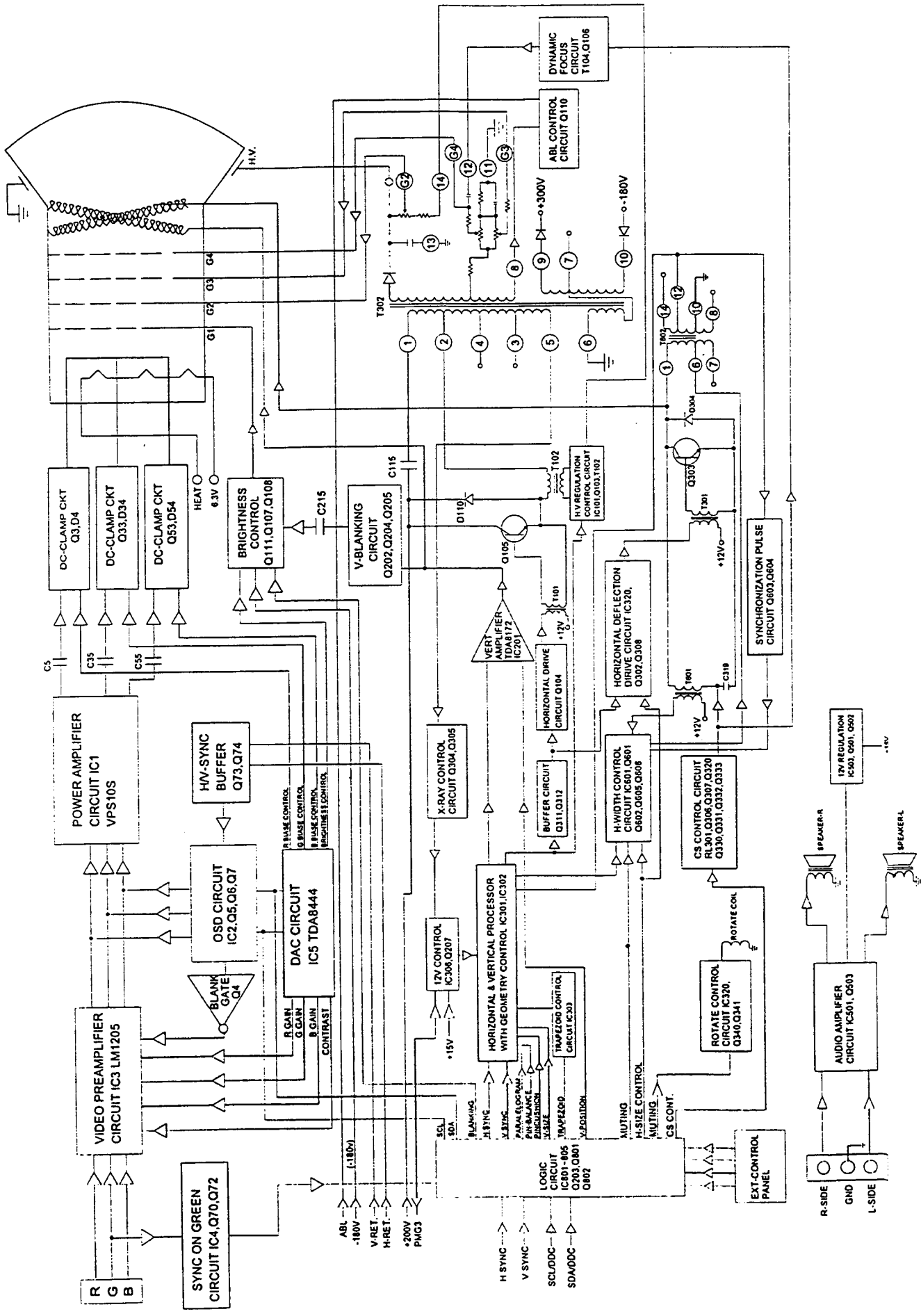


Figure 3-2 Video,Logic,Audio and Deflection Block Diagram

(Voltage Controlled Oscillator). This technique allows autosync operation over the entire frequency range using just one optimized set of external components.

The system includes a second phase detector which compensates for storage time variation in the horizontal output transistor, the picture's horizontal position is thus independent of temperature and component variance.

The LM1291 provides DC control pins for H drive duty cycle and flyback phase.

3.2.2. IC301 LM1291 Pin Descriptions

Pin 1 Clamp Control:
This low impedance current mode. When there is no H sync in sync-tip mode, the clamp pulse is generated by the VCO at the frequence preset by pin 5. This feature is intended for use in on screen display system.

Pin 2 Clamp pulse:
Active -low clamp pulse output.

Pin 3 Video Mute:
This open-collector output produces an active-low pulse when triggered by a step change of H sync frequency.

Pin 4 F-Max:

A resistor from this pin to ground sets the upper frequency limit of the VCO.

Pin 5 F-Min:
A resistor from this pin to ground sets the lower frequency limit of the VCO.

Pin 6 Voltage Refer CAP:
This is the decoupling pin for the internal 8.2V reference.

Pin 7 VCC:
12V nominal power supply pin.

Pin 8 Vertical Sync In:
This pin accepts AC-coupled vertical sync of either polarity.

Pin 9 Composite Video In:
The composite video sync stripper is active only when no signal is present at pin 12 (H/HV In). The signal to pin 9 must have negative going sync tips which are at least 0.14V below black level.

Pin 10 H/HV CAP:
A capacitor is connected from this pin to ground for detecting the polarity and existence of H/HV sync at pin 12.

Pin 11 H/HV Sync Out:
The sync processor outputs active-low H/HV sync derived from the active sync input (pin 9 or pin 12). Pin 11 stays low in the absence of sync input.

Pin 12 H/HV Sync In:
This pin accepts AC-coupled H or composite sync of either polarity.

Pin 13 H/HV Pol Out:
A low logic level indicates active-high H/HV sync to pin 12, a high level indicates active-low. Pin 13 stays low in the absence of H/HV sync.

Pin 14 H Drive Duty Control:
A DC voltage applied to this pin sets the duty cycle of the horizontal drive output (pin 20) . With a range of approximately 30%~70%. 2V sets the duty cycle to 50%.

Pin 15 H Drive EN:
A low logic level input enables H-Drive out (pin 20).

Pin 16 X-ray Shut Down:
This pin is for monitoring CRT anode voltage. If the input voltage exceeds an internal threshold. H-Drive out (pin 20) is latched high and video mute (pin 3) is latched low. Vcc has to be reduced to below approximately 2 V to clear the latched condition, i.e power must be turned off.

Pin 17 Vertical Sync Out:
The sync processor outputs active-low vertical sync derived from the active sync input (pin 8, pin 9 or pin 12). Pin 7 stays low in the absence of sync input.

Pin 18 Flyback In:
Input pin for phase detecor 2. For best operation, the flyback peak should be at least 5 V but not greater than Vcc. A pulse width greater than 1.5μs is acceptable.

Pin 19 Vertical POL Out:
A low logic level indicates active-high vertical sync to pin 8, a high level indicates active-low. Pin 19 stays low in the absence of vertical sync.

Pin 20 Horizontal Drive Out:
This is an open-collector output which provides the drive pulse for the high power deflection circuit. The pulse duty cycle is controlled by pin 14.

Pin 21 Ground:
System ground. For best jitter performance, all LM1291 filter components and bypass capacitors should be connected to this pin via short paths.

Pin 22 Phase Detector 2 CAP:
The low-pass filter cap for the output of phase detector 2 is connected form this pin 21 (GND) via a short path.

Pin 23 Horizontal Drive Phase:
A AC control voltage applied to this pin sets the phase of the flyback pulse with respect to the leading edge of horizontal sync.

Pin 24 Vertical CAP:
A capacitor is connected from this pin to ground for detecting the polarity and existence of vertical sync at pin 8.

Pin 25 FVC CAP 2:
Secondary FVC filter pin. Cfvc 2 is connected from this pin to ground. The width of the video mute (pin 3) pulse is controlled by the time constant difference between the filter at pins 25 and 26.

Pin 26 FVC CAP 1:
Primary FVC filter pin. Cfvc 1 is connected from this

pin to pin 21 (GND) via a short path. The voltage at this pin is buffered to pin 27 (FVC out).

Pin 27 FVC Out:
Buffered output of the frequency-to-voltage converter, which sets the VCO center frequency through an external resistor to pin 28. Care should be taken when further loading this pin, since during the vertical interval it presents a high output impedance. Excessive loading can cause top-of-screen phase recovery problems.

Pin 28 PD 1 Out/VCO In:
Phase detector 1 has a gated charge pump output which requires an external low-pass filter. For best jitter performance, the filter should be ground to pin 21 (GND) via a short path. If a voltage soucrce is applied to this pin, the phase detector is disabled and the VCO can be contorlled directly.

3.2.3. IC302 LM1295 DC Controlled Geometry Correction System

The LM1295 is specifically designed for use in a continuous sync monitor. The injection-locked vertical oscillator operates from 50 Hz to 170 Hz, covering all known video monitors. A differential ouptut current is provided in order to prevent ground interaction.

The IC302 provides two outputs composed of the summation of DC controlled 1st and 2nd order ouptut terms. The first ouptut corrects for EW pincushion and trapezoid. The second corrects for parallelogram and bow.

A DC controlled output is provided for vertical dynamic focus correction.

3.2.4. IC302 LM1295 Pin Descriptions

Pin 1 Ground:
This pin should be connected to the power ground at pin 17.

Pin 2 Vertical Height:
A Voltage between 0V and 4V on this pin controls the amplitude of the +V and -V drive currents, with increasing voltage giving increasing current. The control range is approximately 1.8 to 1. The response time is low, being limited by the automatic level control loop.

Pin 3 4V CAP:
A C202 capacitor aluminum electrolytic or tantalum, should be connected between pin 3 and GND to bypass the internal 4V reference.

Pin 4 Vertical Sync In:
The vertical sync input takes a negative-going TTL level pulse which injection locks the vertical oscillator to the vertical sync frequency if it is above the LM1295 minimum frequency. The minimum pulse width is approximately 200µs. For free-running detection (no vertical sync in), this input should be at logic high.

Pin 5 8V CAP:
A C203 capacitor, aluminum electrolytic or tantalum, should be connected between pin 5 and GND (pin 17) to bypass the internal 8V reference.

Pin 6 Vertical Dynamic Heigh:
A voltage between 3V and 4V on this pin controls the amplitude of the +V and -V drive currents with increasing voltage giving increasing current. The control range is approximately 1.3 to 1.

Pin 7 Vcc:
Vcc should be bypassed to GND (pin 17) with a C216 aluminum electrolytic or tantalum capacitor. The supply voltage is 12V.

Pin 8 Voltage Reference CAP:
A C217 capacitor aluminum electrolytic or tantalum, should be connected between pin 8 and GND (pin 17).

Pin 9 Horizontal Dynamic width:
This output consists of the sum of the vertical ramp and the parabola derived from the ramp. The amplitude and polarity of the ramp signal is DC controlled by horizontal trapezoid control (pin 11) and of the parabola by E-W pin control (pin 10). The weighting of lthe ramp is 1/3 the parabola; i.e, with the horizontal trapezoid and E-W pincushion controls at 4V, the output is 3 parts parabola and 1 part ramp. Horizontal dynamic width is used to correct for trapezoid and east-west pincushion distortion.

Pin 10 E-W Pincushion Control:
A voltage of 0V to 4V adjusts the polarity and the amount of parabola in the horizontal dynamic width (pin 9) output. At approximately 2V, the amount is zero. From 2V to 4V, the amplitude increases and the parabola is positive-going. From 2V to 0V, the amplitude increases and the parabola is negative-going.

Pin 11 Horizontal Trapezoid Control:
A voltage of 0V to 4V adjusts the polarity and the amount of vertical ramp in the horizontal dynamic width (pin 9) output. At approximately 2V, the amount is zero. From 2V to 4V, the amplitude increases and the ramp is positive-going. From 2V to 0V, the amplitude increases and the ramp is negative-going.

Pin 12 Horizontal parallelogram control:
A voltage of 0V to 4V adjusts the polarity and the amount of vertical ramp in the horizontal dynamic center (pin 14) output. At approximately 2V, the amount is zero. From 2V to 4V, the amplitude increases and the ramp is positive-going. From 2V to 0V, the amplitude increases and the ramp is negative-going.

Pin 13 Horizontal Bow Control:
A voltage of 0V to 4V adjusts the polarity and the amount of parabola in the horizontal dynamic center (pin 14) output. At approximately 2V, the amount is zero. From 2V to 4V, the amplitude increases and the parabola is positive-going. From 2V to 0V, the amplitude increases and the parabola is negative-going.

Pin 14 Horizontal Dynamic Center:
This output consists of the sum of the vertical ramp and the parabola derived from the ramp. The amplitude and polarity of the ramp signal is DC controlled by horizontal parallelogram control (pin 12) and of the parabola by horizontal bow control (pin 13). The difference between

this output and the horizontal dynamic width output is in the weighting of the ramp, which is equal to the parabola; i.e with the horizontal parallelogram and horizontal bow controls at 4V, the output is 1 part parabola and 1 part ramp. Horizontal dynamic center is used to correct for parallelogram and bow distortion.

Pin 15 Vertical Dynamic Focus Control:
A voltage of 0V to 4V adjusts the polarity and the amount of parabola in the vertical dynamic focus (pin 16) output. At approximately 2V, the amount is zero. From 2V to 4V , the amplitude increases and the parabola is positive-going. From 2V to 0V, the amplitue increases and the parabola is negative-going..

Pin 16 Vertical Dynamic Focus:
This output consists of the parabola derived from the vertical ramp. The amplitude and polarity are controlled by vertical dynamic focus control.

Pin 17 Ground:
This is the power supply ground for the 12V supply and the point to which the bypass capacitors are returned.

Pin 18 Automatic Level Control CAP:
This capacitor (C204) is part of the level control circuit that maintains constant vertical height in spite of vertical sync frequency changes. If the VCO capacitor value is changed, the capacitor value should change in the same ratio. A R204 resistor should be connected from this pin to ground.

Pin 19 Double Frequency Capacitor:
This capacitor (C218) prevents the vertical oscillator from locking at twice the vertical sync frequrncy. If the VCO capacitor volue is changed, this capacitor value should change in the same ratio.

Pin 20 Oscillator Capacitor:
This is the vertical oscillator capacitor (C232). The value can be changed to change the minimum frequency.

Pin 21 Vertical Resistor:
One end of the vertical resistor connects to this pin. This resistor determines the gain of the vertical ramp current generator. The gain is inversely proportional to the resistance.

Pin 22 Vertical Resistor:
The other end of the vertical resistor connects to this pin.

Pin 23 Vertical Drive:
This is the negative-going vertical ramp output current of the differential pair. The ramp current waveform is superimposed on a direct current of approximately 315μA. The waveform amplitude is determined by the vertical height (pin 2) control voltage and the vertical dynamic (pin 6) control voltage. The current can be converted into voltage by a R236 resistor to ground or by a differential amplifier using the differential currents as inputs. The voltage compliance of the output is typically 6V.

Pin 24 + Vertical Drive:
This is the same as vertical drive except it is the positive-going output current of the differential pair.

3.2.5. Vertical Deflection Circuit

1. IC202 TDA8172 consists of a flyback generator, voltage stabilizer, drive circuit and vertical output amplifier.

2. **The vertical oscillator circuit**

   (a) The frequency and phase of the vertical oscillator circuit is generated by the vertical synchronization signal.

   (b) The synchronization signal is input from Pin 4 of IC302 LM1295, and after being processed by the synchronization circuit, is sent to the vertical synchronization oscillator circuit to trigger the vertical oscillator and synchronize the oscillator frequency with the external synchronization signal. The frequency of its internal free oscillation is set by the time constant of C232. It does not need an external F/V control because this IC302 can keep vertical synchronization. Pin 18 provides vertical A.L.C function. So the pin 18 of IC302 is use to maintain the difference between the free oscillation frequency and external synchonization signal frequency at a similar level and make the sawtooth wave amplitude from pin 24 of IC302 the same.

3. **Vertical Size Control**

   The pulse voltage output by the oscillator is sent to the sawtooth wave generator. The size and amplitude of the voltage of the sawtooth wave generation can be changed by DC value which output from Pin 35 (PWM) of IC801 and the vertical size can thus be controlled. This sawtooth wave voltage passes through a buffer and is output from Pin 24 of IC302 to pin 1 of IC201 TDA8172 of the vertical drive circuit.

   The vertical ramp and DC offset are also controlled by PWM output. The vertical ramp generated across C232 is buffered internally to IC302 by DC controlled variable gain stage. The voltage level is derived from pin 35 (PWM) through the R210, R206 and C206 of grneration, then into pin 2 of IC302.

4. **Vertical Drive Circuit**

   (a) It is not sufficient to rely solely on the oscillator circuit output to ensure the stability of the vertical output, so a first or second level amplifier circuit must be inserted between the oscillator circuit and the output. This circuit is called the drive amplifier and in addition to amplifying the sawtooth wave also corrects the vertical linearity.

After adding the drive circuit, because the level of amplification can be considerable, enough negative feedback can be added to correct vertical linearity and increase the stability of the circuit.

(b) If the current of the sawtooth wave flowing through the deflection yoke is distorted, then the top and bottom portions of the display will be expanded or compressed, resulting in poor linearity. In order to solve this problem, correction of the linearity of the sawtooth wave can be carried out before the drive level.

5. **IC201 TDA8172 Vertical Drive Circuit**

The IC201 uses a double power source, so it can be viewed as an OCL drive amplification circuit.

In order that the DC coupled output stage accurate DC reference, a DC reference voltage is taken from pin 5 of IC302. This used as the reference voltage (via divider resistors, R214 and R216) for the DC coupled power amplifier IC201. This is a simple voltage to current inverting amplifier, using R223 to derive a voltage proportional to the current in the deflection winding of the yoke. This voltage is fed back to the virtual signal earth inverting input of the power amplifier(pin1) by R219. This back to back diode feedback network modifies the linearity of the transfer characteristic in order to give precept "S" correction linearity, in addition to the variable correction in the ramp generator.

The vertical output amplifier has a voltage boost circuit to triple the positive supply voltage during retrace in order to speed up flyback. It does this by charging capacitor C210 through diode D202 during the normal forward scan. Pin6 of the IC201 is the voltage supply to the power output stage. When flyback occurs, pin3 is switched to the positive supply rail on pin2, thus adding the voltage across C210 to that of the supply rail, effective doubling the supply momentarily.

6. **Vertical Centering Adjustment**

Since IC201 functions as an OCL circuit, VDC is output from Pin 7 of IC201, so the central current can be changed to shift the on-screen display up or down to prevent voltage fluctuation. After adjusting the power stabilizer at Pin 5 of IC302 LM1295 (about 8V) and R214, R216 this is input to Pin 7 of IC201 to change the value of the vertical center.

The DC operating point of the amplifier can be varied by the pin 38 of IC801 (vertical position) output and via R212, C207 and R213 to pin 7 of IC201 which adds or subtracts an offset into the output, thus varying the DC offset of the scan and hence the vertical centering.

3.2.6. Geometry Correction Circuit

1. If the width of the border in the center of the screen is insufficient, the waveform shown in Figure 3-3 below, can be used to add to horizontal deflection B+ in order to change the deflection of the horizontal deflection circuit. This waveform is the parabola obtained after regulation of the vertical period, and is created to perform amplitude modulation on the horizontal deflection current, as shown in Figure 3-4.

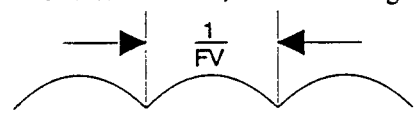
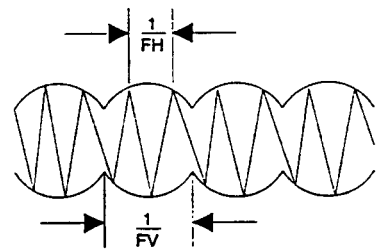


Figure 3-3 Voltage Correction Wave



FH: Horizontal Frequency
FV: Vertical Frequency

Figure 3-4 Current Correction Wave

2. The sawtooth wave is output from Pin 9 of IC302 and through C350 and R364 and input to Pin 2 of IC601 (DC to DC circuit). It is then output from Pin 6 of IC601 and after being sent to T603's second coil output, is added to horizontal B+ to provide pincushion and trapezoid distortion correction. So, is created to preform amplitude modulation on the horizontal deflection output pluse, as shown in figure 3-5.

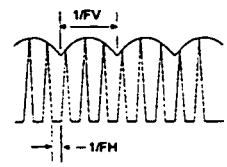


Figure 3-5 Collector of Q303 Output Pluse Correction Wave

3. The sawtooth wave is output from pin 14 of IC302 and through R353 and C314 and input to pin 23 of IC301. It is added to horizontal phase to provide parallelogram and bow distortion correction.

3.2.7. Structure of Horizontal Deflection Circuit

The function of the horizontal deflection circuit is to cause left/right scanning of the electron beam using the sawtooth wave current flowing through the horizontal deflection yoke, and is made up of the hori-

zontal oscillator circuit, horizontal drive circuit, horizontal output circuit, synchronous AFC circuit and high voltage generator circuit.

1. **Horizontal Drive Amplifier**
In order to rapidly saturate the output transistor (ON) or cut it off (OFF), a sufficient basic current must be provided. Because of this, an amplifier circuit is added between the oscillator circuit and the output circuit to amplify the pulse voltage. At the same time, after the waveform has been regulated, by adding this circuit to the output circuit, this amplification circuit functions as a drive amplifier.

IC301 LM1291 consists of a vertical sync selection polarity circuit, composite video sync stripper circuit, AFC circuit, H/V sync and composite sync circuit, voltage control oscillator circuit, phase regulator circuit, X-Ray circuit, video mute circuit, voltage regulator circuit and horizontal drive duty cycle circuit. This IC includes the vertical and horizontal circuits combined in one package.

When the synchronization signal input to logic circuit and pin 12 of IC301. The pin 20 of IC301 output horizontal frequency is achieved by the pin 1 of IC801 and flyback pulse from pin 12 of T602 (A.F.C) fed to pin 18 of IC301. So , the pin 20 of IC301 output horizontal frequency through Q311, Q312, Q302, Q104 T101 and T301 provide a horizontal output transistor base current of Q303 and horizontal anode voltage generator output transistor base current of Q105.

The horizontal output transistor base drive is taken from a conventional base drive transformer stage. This circuit as in a similar manner to a flyback power supply. The square wave horizontal oscillator output signal is coupled into the base of emitter drive stage transistor Q302, Q104, T301, T101 across the +15V supplies. This causes the primary current to increase linearly until such time as Q302 and Q104 turns off, hence storing a predetermined amount of flux energy in the transformer. As Q302 or Q104 turns off, and the primary current falls to zero, the secondary voltage is driven above the threshold of the base-emitter junction voltage of the horizontal output transistor Q303 or Q105. Current flows through R320, R321, L301, L302 and D303 into the base of Q303 or through R116, R150, L101 and D130 into the base of Q105 hence turning this device on. The high base current of around 1.1A. Lamps is so high that Q303 or Q105 is driven heavily into saturation. This is important in order that the collector voltage should be as low as low as possible whilst conducting the high peak currents that flow through the horizontal deflection winding. In turn, this is vital to limit dissipation.

At the required time as determined by the horizontal oscillator, the base drive transistor is turned back on. The voltage at Q302 or Q104 collector fall rapidly back towards the ground rail. However, the secondary current still remains flowing in a positive direction for a short time, due to the finite leakage inductance of T301 or T101. Also, due to the heavy saturation of Q303 or Q105, the base voltage remains at around 1V. The current in the secondary winding rapidly reverses and goes sharply negative as the charge stored within the base region of Q303 or Q105 is removed. D303 or D130 helps to speed up this charge removal. Note that during this time, the collector output of the Q303 or Q105 is still turned on, even though the base current is flowing out of the base.

This period of time is known as the storage time of the device and may take between 2-3us, depending upon peak collector current and temperature and various other design factors. Finally, when all charge in the base region of Q303 or Q105 is dissipated the base current suddenly stops, and the secondary current drops almost instantly to zero. At that point, the device now become non conducting and the collector current flow also terminates. The secondary voltage on T301 or T101 drops to it's unloaded voltage and the current flow in the primary settles to it initial value once more.

2. **Horizontal Equivalent Output Circuit**
The horizontal output circuit uses the switch operation of a transistor and a damping diode, and provides a sawtooth wave current to the deflection yoke. The horizontal deflection yoke is made up of the L value on the coil and resistance r inside the coil connected in series. Its resistance is extremely small, and the time constant (L/r) is extremely large. Because of this the voltage at the two terminals of the coil cause rapid variation in the current flowing in the coil still will slowly vary, creating a sawtooth current. The basic circuit and equivalent circuit are shown in Figures 3-6 and 3-7.

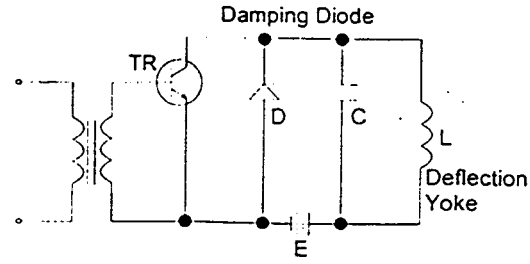


Figure 3-6 The Basic Deflection Circuit

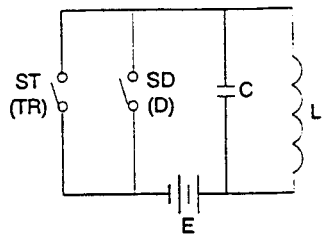


Figure 3-7 Equivalent Circuit

3. **Horizontal Output Equivalent Circuit Operation**
Refer to Figure 3-8 for the current wave of the voltage of the horizontal output circuit during operation.

(a) t1 — t2 Period
The base of the output transistor is added to the forward bias voltage. As the current through the base is very large, it will cause the output transistor to be saturated, corresponding to the ON state of S1 in the equivalent circuit. At this time the deflection yoke contains a current flow and because the time constant is large, the current will slowly show a linear increase as shown in Figures 3-8 (b) and 3-9 (a).

(b) t2-t3 Period
At t2, a negative load is applied to the to the base and the output transistor changes to OFF (S1 in open state). There is no current passing through the transistor at this time and the L and C components of the deflection yoke become independent oscillation circuits. If the current is suddenly cut off, then the polarity of the inverse voltage generated at L will be as shown in Figure 3-9 (b). This voltage is viewed as the source voltage and will cause current to flow, at which time the current flowing to C is as shown in Figure 3-8 (d). At time t3 this current is 0 but the voltage at the two capacitor terminals is at maximum. This waveform is known as flyback pulse, and is shown in Figure 3-8 (f).

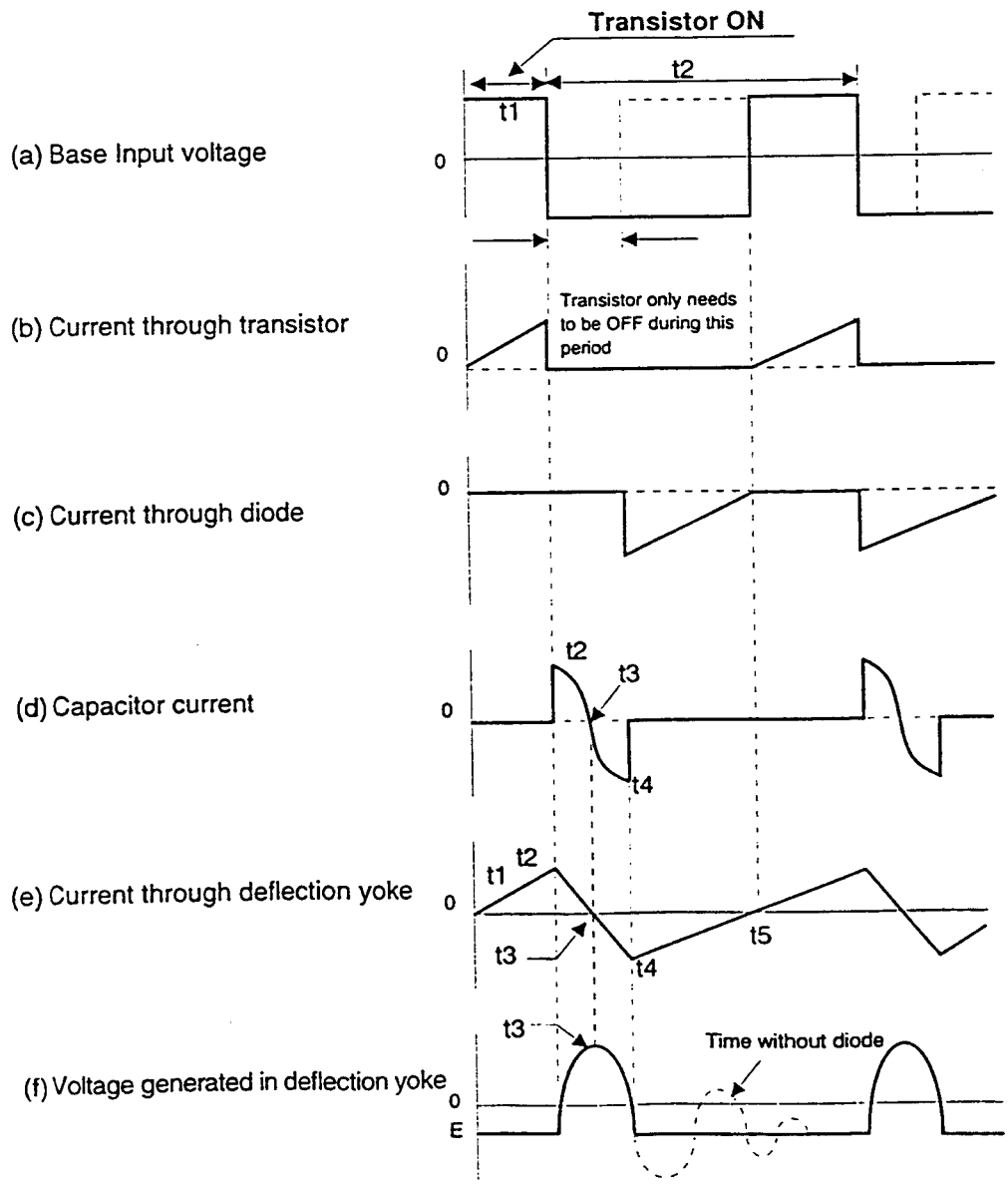
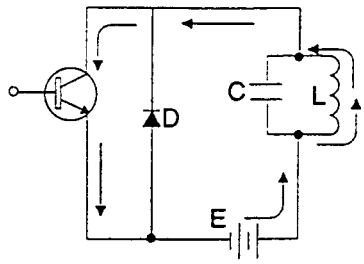
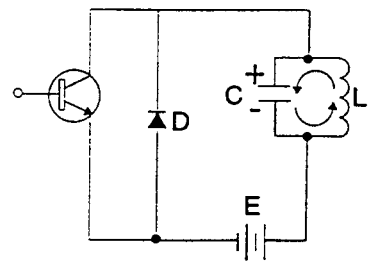


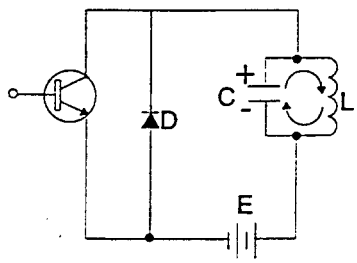
Figure 3-8 Horizontal Output Voltage/Current Waves



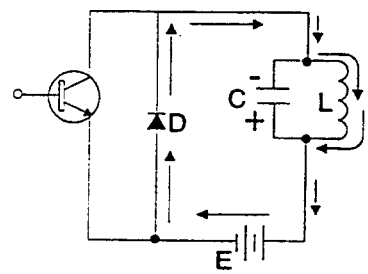
(a) Second half of scanning period (t1 - t2)



(b) First half of return line period (t2 - t3)



(c) Second half of return line period (t3 - t4),



(d) First half of scanning period (t4 - t5)

Figure 3-9 Polarity of Transformer Voltage

(c) (t3 — t4) Period

The energy accumulated in C is released to the deflection yoke, the direction of the current flow being shown in Figure 3-9 (c). The current increases as the voltage on C decreases, and at time t4, the voltage of C is 0, at which time the current is at maximum, which means the current flowing into the deflection yoke is also maximum. C is then charged and if a damping resistor is not connected, the energy between L and C will be reversed, which is the oscillation frequency set by the oscillator at L and C.

(d) t4 — t5 Period

At t4, the voltage of C is 0. After this it is recharged in the opposite direction and this voltage exceeds the voltage of the power source at time t4. At this time the damping diode is ON and the L and C circuits are shorted out and stop oscillating. Because of this the time constant of r and L in the damping diode is large so the current flowing in the deflection yoke does not suddenly become 0. The current shows a linear decrease, and when it becomes 0 at time t5 the transistor is ON and the operation described above is repeated.

As described above, the current flowing in the deflection yoke during scanning is the sum of the current which has passed through the transistor and the damping diode current. Please refer to Figure 3-8 (e).

4. **Horizontal output operation:**

The actual output stage differs from the simple model described in a number of ways. Refer to the basic schematic of the major components in Figure 3-10 on the following page.

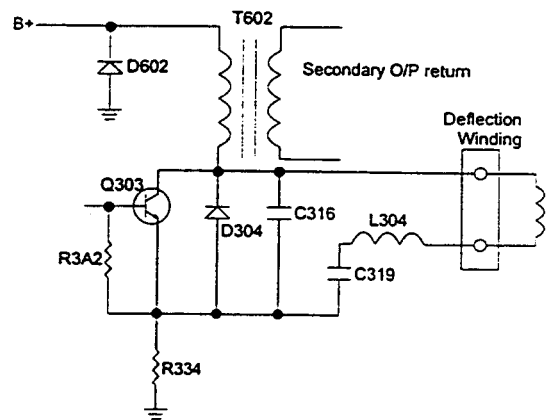


Figure 3-10 Basic Horizontal Deflection Output Circuit

The main inductance L is now divided into the primary winding of the Flyback Transformer (FBT) T602 and the deflection yoke winding. The deflecting yoke is coupled through a capacitor C319, which has two function. Primarily it prevents DC unwanted DC currents flowing through the deflection yoke which would otherwise cause an undesirable deflection of the CRT beam.

Secondly, the voltage drop across it due to the AC ramp current flowing causes a parabolic modulation in the slope of the ramp, leading to a progressive curve in the ramp, symmetrical about the zero current value as shown in Figure 3-11. This intentional distortion of the linear ramp is required to compensate for the 'S', or symmetric linearity distortion in the CRT.

In series with C319 and the deflection yoke is another indicter, L304. This is a saturating indictor that is biased with a permanent magnet.

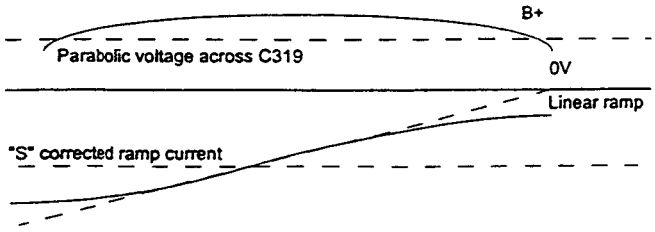


Figure 3-11 Linear Ramp Distortion

Consequently this device has a linearity that is higher for current flow in one direction than in the opposite direction. This function provides compensation for resistive losses that would otherwise cause an undesirable exponential curve to the linear ramp, resulting in asymmetrical linearity errors in the displayed image.

The voltage seen in the output stage require special attention. The B+ supply can varying between 60-180V. The main flyback pulse seen across Q303 and associated components is around 1100Vp. Consequently, appropriate precautionary measures must be taken when servicing the monitor.

In addition to the basic topology as described above, there are a number of other additional devices. Q306, Q307, Q303 and Q333 can be independently turned on or off under logic control. These devices switch addition capacitors, C320, C322, C362 and C367 in parallel with C319 to alter the amount of 'S' correction at different horizontal scan frequencies.

D308 and D309 acts as a constant current source that can be under SW301 control. This current source drives an adjustable constant current into L304. This current flows into the deflection yoke and adds a variable DC offset to allow image raster centering to be achieved.

The B+ provides current for the deflection coil (D/Y). Therefore, changes in deflection current can be controlled by modifying B+ voltage. As a result, horizontal width can be modified. In order to obtain the side horizontal width for different frequencies, a DC to DC feedback circuit is added. The synchronization signal comes from deflection output, from pin 12 of T602 to base of Q603 which drives Q604 to trigger pin 4 of IC601. Feedback signal come from secondary on T601, via D604, R611 and R612 to become a DC voltage on pin 2 of IC601, another feedback signal passes through emitter of Q303, via R606 on pin 3 of IC601. There signals determine duty cycle of output signal of IC601 which is coupled to T603 to drive Q601, to control B+, making it possible to have correct deflection current and horizontal width on different frequencies. Similarly, output pin 36 of IC801 drive through R368, C348 and R610 to control duty cycle of IC601 output to achieve horizontal width adjustment.

During mode change, the B+ supply can be instantly turned off by pulling up the error amplifier input on pin 1 of IC601. These can be achieved by Q602, Q606 and Q605 which is driven from the logic circuit pin 9 of IC801 (MUTE). Whilst Q602, Q606 and Q605 can switch off the B+ supply almost instantly, the time taken for the supply to restart is programmed by the value of logic circuit.

In addition, the B+ (200V) supply is configured so as to maintain a constant anode voltage. The anode voltage is derived from the flyback transformer T103. As the flyback voltage across the primary is already a high voltage pulse of around 800Vp, it requires only a modest turns ratio to step this pulse up to around 26kV, the working voltage of the CRT. Refer to the basic schematic of the major components in figure 3-12.

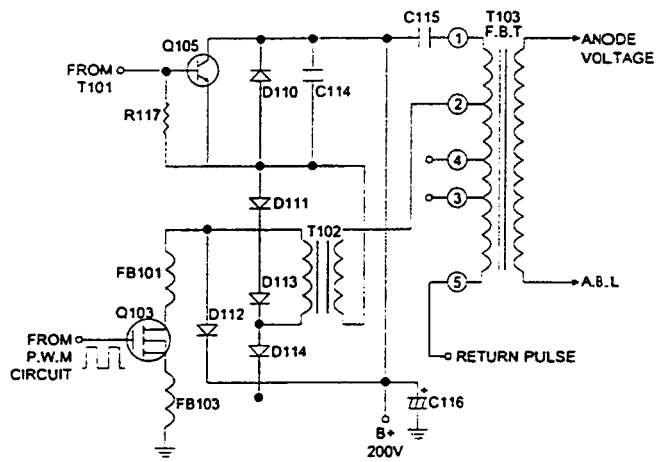


Figure 3-12 Basic High Voltage Output Circuit

The flyback pulse at the primary of T103 is proportional to the both frequency and the supply rail B+. In order to maintain the anode voltage at a constant 26kV a regulation system is required. This is achieved using a PMW regulation stage formed by a IC101 driving a Q103. The causes a regulating current on primary T102, the voltage changes in secondary T102 result in a constant high voltage, synchronized by the horizontal oscillator. The IC101 has an error amplifier that generates an error signal from the feedback network formed by the high voltage bleed resistor and capacitor (it is internal to T103). Resistors VR101, R103 and R104 set the DC feedback ratio, and by adjustment of VR101, this ratio can be adjusted at setup to set the high voltage at it's nominal value of 26kV. The AC frequency response of the serve loop is set by C104, D103 and D104 for optimum stability and relegation characteristics.

The output of the error amplifier which can be observed on pin 1 of IC101 is internally compared with a DC voltage. This DC is produced across.

The average beam current through the CRT also flows through the secondary high voltage winding of T103 connected to pin 8 of T103, C132 and R138 smooths the pulse of current flowing in the secondary winding and the average DC current is supplies through resistor R137 and VR106. When the average secondary current flowing exceed 460mA, this voltage begins to drop below this threshold. Thus a signal is generated which can be fed to video amplifier for automatic beam current limiting (ABL).

3.2.8. X-RAY Protection Circuit

The feedback pulse voltage from T103 F.B.T is regulated through D302 to obtain a DC voltage and the appropriate set voltage is distributed by R323 and R324. When the feedback pulse voltage exceeds the set voltage, a DC voltage develops in the cathode of ZD302 which turns on Q304 and Q305. As a result, the pin 1 of IC306 (adj-pin) to 0V, so IC306 is turned off, putting the 12V is not output. This is the phenomenon of high voltage protection.

3.2.9. The Focus Circuit

The output waveform come from pin 16 of IC302 through C122 and R123 to the amplifier Q106, via T104 with horizontal waveform to modulation. After, the wave coupling of the T103 which make the focus performance on the C.R.T. This is waveform shown in figure 3-13.

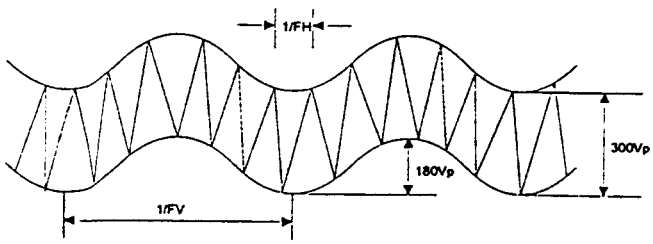


Figure 3-13 Focus Correction Wave

3.2.10. Horizontal linearity and CS Switching

Switching CS is necessary to ensure the lines are in accordance with the specifications in multi-sync monitors.

- For frequencies 69.5~85kHz, Q307 and Q333 are OFF and RL301 is ON so CS is only C319, but L304 and L305 in parallel.
- For frequencies 55~69.5kHz, Q307 and Q333 are OFF, RL301 and Q330 are ON, so CS are C319 and C362 in parallel, but L304 and L305 are in parallel.

Truth Table of Frequency Discriminator						
FEQ CS	30~34 kHz	34~39 kHz	39~45 kHz	45~55 kHz	55~69.5 kHz	69.5~85 kHz
CS1	L	L	L	H	H	H
CS2	L	L	L	L	H	H
CS3	L	L	H	L	L	H
CS4	L	H	H	H	H	H

Truth Table of Power Saving Detector						
Mode	H-sync	V-sync	PMG1	PMG3	Mute	Blanking
ON	Pulse	Pulse	1	0	0	0
Standby	No Pulse	Pulse	1	1	1	1
Suspend	Pulse	No Pulse	0	1	1	1
OFF	No Pulse	No Pulse	0	1	1	1

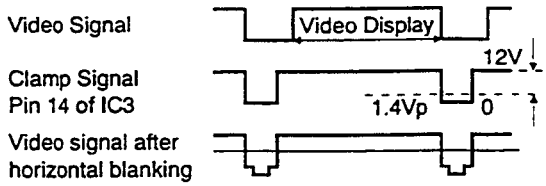
- For frequencies 45~55kHz, Q333 is OFF, RL301, Q307 and Q330 are ON, so CS are C319, C322 and C362 in parallel, but L304 and L305 are in parallel.
- For frequencies 39~45kHz, RL301, Q330 and Q333 are OFF and Q320 is ON, so CS are C319, C320 and C322 in parallel, but linear coil is only L304.
- For frequencies 34~39kHz, RL301and Q333 are OFF, Q307 and Q330 are ON, so CS are C319, C320 C322 and C362 in parallel, but linear coil is only L304.
- For frequencies 30~34kHz, RL301is OFF, Q307, Q330 and Q333 are ON, so CS are C319, C320, C322, C362 and C367 in parallel, but linear coil is only L304.

3.3. Video Amplifier

The RGB video and sync signals are supplied through a video cable directly to the Video Board at connector P1. The RGB signals are terminated in 75 ohms by R1 and R31, R50 and R51.

The RGB signals then enter an IC3 LM1205 video pre-amplifier, providing synchronous black level clamping, variable picture contrast (gain) and RGB gain balance for alignment. Separate gain control voltages for the three pre-amplifier channels are provided via R67, R47 and R17 from the IC5 TDA8444 DAC which is loaded by the microcontroller via the I2C bus. These inputs enable the individual gains of each channel to be varied to allow channel gain balance. In addition, a common signal is applied on pin12 of IC3 to adjust all three channels by the same amount, to allow for overall gain or contrast control.

A synchronous clamping signal is derived from the horizontal sync pulse by Q2. This takes the trailing edge of the horizontal sync pulse, differentiates it through C74 and R82, which is applied pin 14 of IC3. The timing is shown in Figure 3-14.



NOTE:

A. Clamp signal is generated from horizontal sync pulse time.

B. When the Clamp signal is less than 1.4Vp-p, the IC's internal clamp loop will operate; when greater than 1.4Vp-p, it will not operate.

Figure 3-14 Timing of Pin 14 Clamp Signal

The outputs of the video pre-amplifier are fed to IC1, a hybrid power amplifier IC type VPS10S, through resistors R6, R36 and R56. In addition, on screen display video information generated by IC2 can be injected via Q5, Q6 and Q7 through R3, R33, R53 and D83, D84, D85.

IC1 amplifies the video signals to around 40Vp-p. The outputs are AC coupled to the CRT cathodes via C5, C35 and C55. In order to bias the DC level of the cathodes correctly, the AC coupled signal is DC restored by clamping to a DC voltage which can be varied under microprocessor control. Considering Red channel output on IC1 as an example, the signal is clamped by D4 to the voltage set by the transistor amplifiers formed by Q3, which amplify the adjustable voltage at the output of the DAC. A similar stage can be seen for the green and blue channel outputs.

When the RC video signal amplification circuit is added for amplification, this waveform will change as shown in Figure 3-15 (a). Without the DC component, as shown in Figure 3-15 (b), the DC level of darker and brighter displays will be different,so when this kind of signal without a DC component is sent to the CRT, it will cause the contrast of the image to change as the signal changes. Therefore Q3 and D4 serve as a DC clamp and the CRT's cathodes DC voltage can be adjusted by the IC5 TDA8444 DAC.

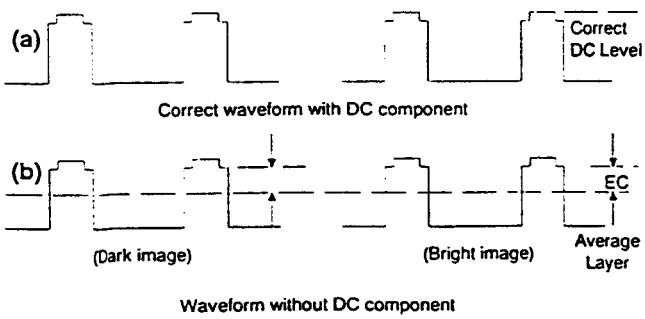


Figure 3-15 The Post Output Amplifier Circuit

IC2 is an On Screen Display processor. This is a simple video generation IC2 that has its own oscillator circuit. The oscillator circuit by using an internal Phase Locked Loop (PLL) the IC2 can sync to the incoming vertical and horizontal oscillator frequencies and produce the OSD video signals once initialized and loaded by the commands and data received on the I2C bus. When the OSD display is activated, the blanking output of the IC2 also sends a signal to the blanking input of IC3 (pin13) to provide an optional black background for the OSD display.

The RGB signals are amplified to drive the CRT by an IC1 VPS10S hybrid amplifier and capacitively coupled to the cathodes.

Brightness control is achieved by varying the bias of G1 of the CRT via a transistor stage formed by Q111 which is also driven by an output of the pin 9 of IC5. Vertical blanking signals is coupled into this amplifier Q204, Q205 and Q202 to prevent visible retrace lines.

3.4. Microprocessor And Sync Processing

The microprocessor is a MC68HC705BD3P type It is particularly suitable as multisync computer monitor controller. This 8-bit microcontroller unit (MCU) contains an onchip oscillator, CPU, RAM, ROM, M-Bus serial interface system (IIC), parallel I/O, Pulse Width Modulator, Multi-Function Timer and sync Signal Processor. It has a 7.75k bytes of ROM and 256 bytes of RAM on internal which contains a basic communication 'boot' routine and various other simple routines. It is also used to store the OSD icon bit map. The main firmware routines and variable data stored in the 16k external EEROM, IC802.

When the micro is instructed via the IC2 bus, the internal ROM boot routine will load up the EEROM with program data from the IC2 bus. Thus it can be made to load its own firmware. From then on it will run jointly out of EEROM and internal ROM. Another important routine within the internal ROM is the routine which allows data writes to be made to the EEROM. This must be resident in the micro as it cannot run from the EEROM whilst writing data. These control the addressing and I/O port selection from the micro CPU in the IC801 (MC68HC705BD3P).

Also specialized ports Pin16, Pin 17 and Pin18 of IC801 form the M-Bus interface which is used internally to set the DAC valuse and the OSD IC and CS table control IC (IC803). Other way, specialized ports pin 11 and pin 12 of IC801 from the M-bus interface which is used internally to set the data to external EEROM IC802. In addition, the I/O ports from pin 19 to pin 23 of IC801 from the M-bus interface which is used internally to set the front panel control.

There are 16 PWM channel. Channel 0 to channel 7 are dedicated PWM channels while channel 8 to channel 15 are shared with ports C under the control of the corresponding configuration register. Thus it can be made to control H-PHASE, PARALLELOGRM, PIN-BALANCE, TRAPEZOID, PINCUSHION, TILT, V-SIZE, H-SIZE and V-POSITION on the pin 1, pin 26, pin 27, pin 28, pin 29, pin 34, pin 35, pin 36, pin 37 and pin 38 of IC801.

The micro also drives the sync selection circuits. IC801 is used to set the polarity of the incoming sync signals and allows the micro to sample the vertical and horizontal syncs and to select the correct polarity on the outputs H-SYNC and V-SYNC appropriately. In addition, whilst sampling the polarity, the micro can measure the frequency of both syncs. By

suitable selection of H-SYNC and V-SYNC control lines, it does this when ever a mode change occurs. A mode change is detected by either a change in vertical frequency, which is monitored by firmware, or by a sudden change in horizontal frequency.

When power is disturbed to the unit, the power reset line goes low. This also causes an input to the micro via the MODEC line. On detecting this interrupt, the micro first checks inputs Pin 4 of IC801. If these are also low, then it knows the MODEC interrupt was caused by an impending power failure. In this case the micro saves the current RAM data in EEROM and prepares for power off. The RESET line is delayed for 7ms by R801, ZD801, R803 and C801 to allow time for the data to be saved. The REST line then holds off the micro and the EEROM until power is good once more.

3.5. Audio Amplifier

IC501 TDA7057AQ consists of a pre-amplifier and power output amplifier circuit.

The R/L audio signals are supplied through a P502 directly to the Main Board at connector to pin 3 and pin 5 of IC501. The separate gain control voltage for the two pre-amplifier channels are provided by VR501. It can providing variable voltage on the pin 1 and pin 7 of IC501. The audio signals output of power amplifier pin 8 and pin 13 of IC501 and via C506 and C507 coupled to the speaker.

Notes

Section 4.
Setup Adjustments

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4.1. Preparing the Display for Adjustment

Before adjusting any the display settings or making final adjustments after service, perform the following pre-test settings to prepare the display for adjustment:

1. Be sure to allow the display to warm up for at least 30 minutes before making any adjustments.
2. When making tests and adjustments, the CRT should be facing east or west to minimize the affect of the earth's magnetic field.
3. Set the contrast control at 80% and the brightness control at 50% for all tests unless otherwise specified.
4. Thoroughly degauss the entire screen with a manual degausser before proceeding with tests.
5. All test should be performed with the rated power supply voltage unless otherwise specified.

4.1.1. Test Equipment Required

The following equipment will be required to make the tests and adjustments detailed in this section:

- ☐ Video signal and pattern generator
- ☐ Digital multimeter
- ☐ Degausser

4.2. Adjustment Procedures

4.2.1. Adjustment Sequence

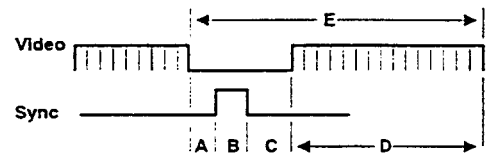
This display undergoes an automatic alignement procedure during manufacture. This alignment procedure follows a fixed sequence of adjustments which are dupplicated in this section. When making manual adjustments during service, you should always make the adjustments in the order given here to ensure correct results.

4.2.2. Preset Timings Used During Adjustment

During alignment it is necessary to input certian preset timings stored in the display. The detailed parameters of all the preset timings are given in the table below for your reference.

IMPORTANT NOTE

The preset timings for different versions of this model may differ from those shown here. Be sure to check the list of preset timings for the unit being serviced.



Mode Number	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7	Mode 8	Mode 9	Mode 10
Data Pixel	1280	1024	1024	800	640	640	800	640	640	640
Data Line	1024	768	768	600	480	480	600	480	400	350
H. Freq.(kHz)	63.980	56.476	48.363	46.875	37.861	37.500	35.156	31.469	31.469	31.469
V. Freq(Hz)	60.010	70.070	60.004	75.000	72.809	75.000	56.250	59.942	70.080	70.080
Pixel Rate(MHz)	110.550	75.000	65.000	49.500	31.500	31.500	36.000	25.175	25.175	25.175
Hor. FP µs(A)	0.434	0.320	0.369	0.323	0.762	0.508	0.667	0.636	0.636	0.636
Hor. Sync µs(B)	1.737	1.813	2.092	1.616	1.270	2.032	2.000	3.813	3.813	3.813
Hor. BP µs(C)	1.882	1.920	2.462	3.232	4.063	3.810	3.556	1.907	1.907	1.907
Hor. Active µs(D)	11.578	13.653	15.754	16.162	20.317	20.317	22.222	25.422	25.422	25.422
Hor. Total µs(E)	15.631	17.707	20.677	21.333	26.413	26.667	28.444	31.778	31.778	31.778
Ver. FP ms(A)	0.032	0.053	0.062	0.021	0.238	0.027	0.028	0.318	0.381	1.176
Ver. Sync ms(B)	0.063	0.106	0.124	0.064	0.079	0.080	0.057	0.064	0.064	0.064
Ver. BP ms(C)	0.563	0.513	0.600	0.448	0.740	0.427	0.626	1.048	1.112	1.907
Ver. Active ms(D)	16.006	13.599	15.880	12.800	12.678	12.800	17.067	15.253	12.711	11.122
Ver. Total ms(E)	16.663	14.272	16.666	13.333	13.735	13.333	17.778	16.683	14.269	14.269
Polarity(H.V)	+,+	-,-	-,-	+,+	-,-	-,-	+,+	-,-	-,+	+,-
Primary mode is 56.476kHz / 70.070Hz (1024x768)										

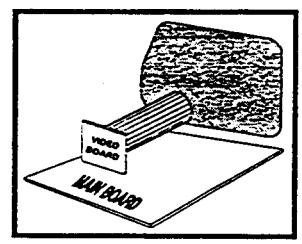
Table 4-1 Table of preset Timing Parameters (original)

Mode Number	Mode 1	Mode2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7	Mode 8	Mode 9	Mode 10
Data Pixel	1280	1024	1024	1024	800	800	640	640	640	640
Data Line	1024	768	768	768	600	600	480	480	480	400
H. Freq.(kHz)	79.976	68.677	61.080	60.023	53.674	46.875	43.269	37.500	31.469	31.469
V. Freq(Hz)	75.025	84.997	75.782	75.029	85.061	75.000	85.008	75.000	59.942	70.080
Pixel Rate(MHz)	135.000	94.500	86.000	78.750	56.250	49.500	36.000	31.500	25.175	25.175
Hor. FP µs(A)	0.119	0.508	0.099	0.203	0.569	0.323	1.556	0.508	0.636	0.636
Hor. Sync µs(B)	1.067	1.016	3.721	1.219	1.138	1.616	1.556	2.032	3.813	3.813
Hor. BP µs(C)	1.837	2.201	0.651	2.235	2.702	3.232	2.222	3.810	1.907	1.907
Hor. Active µs(D)	9.481	10.836	11.907	13.003	14.222	16.162	17.778	20.317	25.422	25.422
Hor. Total µs(E)	12.504	14.561	16.378	16.660	18.631	21.333	23.111	26.667	31.778	31.778
Ver. FP ms(A)	0.013	0.015	0.	0.017	0.019	0.021	0.023	0.027	0.318	0.381
Ver. Sync ms(B)	0.038	0.044	0.131	0.050	0.056	0.064	0.069	0.080	0.064	0.064
Ver. BP ms(C)	0.475	0.524	0.491	0.466	0.503	0.448	0.578	0.427	1.048	1.112
Ver. Active ms(D)	12.804	11.183	12.574	12.795	11.179	12.800	11.093	12.800	15.253	12.711
Ver. Total ms(E)	13.329	11.765	13.196	13.328	11.756	13.333	11.764	13.333	16.683	14.269
Polarity(H.V)	+,+	+,+	+,+	+,+	+,+	+,+	-,-	-,-	-,-	-,+
Primary mode is 60.023kHz / 75.029Hz (1024x768)										

Table 4-2 Table of preset Timing parameters (current)

IMPORTANT NOTE

The adjustment settings in this section are based on REVISION G of the factory alignment procedures. Appendices detailing changes in the factory alignment procedures that have occurred since publication of this service manual are available upon request.



Location of PCBs

Initial settings to be carried out manually prior to automatic alignment:

4.3. High Voltage Verification

1. Input a cross hatch pattern in primary mode and adjust VR101 on the main board (see figure 4-1 for approximate location) so the high voltage is in the range 26kV±0.1.
2. Input a full white pattern in 31.47kHz (640x480) mode. Check that the high voltage is in the range 26kV±0.3.

4.4. G1 Voltage Adjustment

Input a raster pattern (video OFF) in primary mode and push the external brightness control buttern to maximum. Adjust VR102 so that the voltage of G1 read on a digital multimeter is -35V±1 with HITACHI CRT (with TOSHIBA CRT is -45V±1).

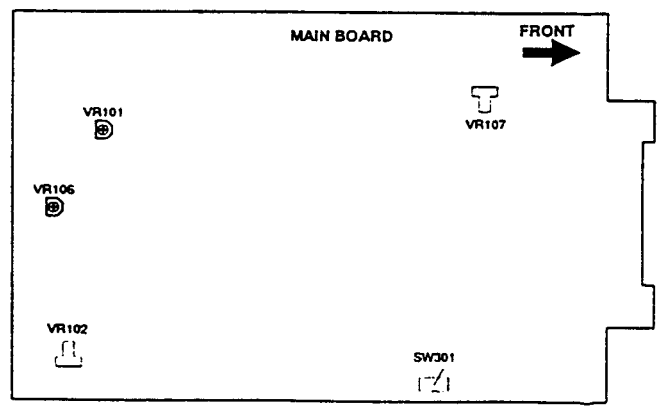


Figure 4-1 Location of on Mainboard

Steps used in white balance adjustment:

4.5. Background Brightness Setting

1. Input a raster pattern in primary mode and push the external brightness control button to maximum. Adjust the SCREEN VR so background brightness is approximately 1.5FL±0.1.

2. Before carrying out white balance adjustment, make sure that the display size and linearity are in spec.
3. Before carrying out white balance adjustment, make sure that the VR106 position shall be turn counterclockwise to the end (ABL no action).
4. Before carrying out white balance adjustment, make sure that the internal contrast VR107 shall be turn to the center position.
5. Input timing in primary mode, and the white balance automatic adjust some item as blow.

   (a) Input no video pattern in primary mode, and set-up brightness of raster white balance get the x,y value is x=0.346±0.01 y=0.359±0.01.

   (b) Input a full white pattern in primary mode, and set-up 5000 degrees kelvin of picture white balance get the x,y value is x=0.346±0.01 y=0.359±0.01.

   (c) Input a full white pattern in primary mode, and set-up 6500 degrees kelvin of picture white balance get the x,y value is x=0.313±0.01 y=0.329±0.01.

   (d) Input a full white pattern in primary mode, and set-up 9300 degrees kelvin of picture white balance get the x,y value is x=0.283±0.01 y=0.298±0.01.

4.6. Screen Brightness Adjustment

1. Input a raster pattern in primary mode. Set external brightness key to maximum and external contrast key to minimum, then make sure that the raster brightness range is 1FL±0.3. If not in this range, adjust screen VR of F.B.T.
2. Input a raster pattern in primary mode. Set external contrast key to maximum and push external brightness key to brightness is 0.08FL, then switch to a display of full white pattern and adjust internal contrast VR107 and check that brightness at the center of the screen is in the range 33FL±1.
3. Input a full white pattern in primary mode. Set external brightness and contrast key to maximum and adjust VR106 and check that brightness at the center of the screen is in the range 36FL±1.

Conclusion White Balance Adjustment:

4.7. Magnetic Field Configuration

Configure the magnetic field as follows:

- ☐ Northern hemisphere : H=0.01, V=0.45
- ☐ Southern hemisphere : H=0.01, V=-0.52

4.8. Raster Center Verification

Input a cross hatch pattern in 79.976kHz (1280x1024) mode, and check raster center shall be less than 3mm (|L-R|≤3mm). If not in this ranged and select SW301 for adjustment raster center.

4.9. Tilt Verification

Input a cross hatch pattern in primary mode and use the tilt rotation key to ensure that tilt is less than 1mm.

4.10. Focus Verification

1. Input a full white pattern in primary mode. Use the external brightness control to adjust background brightness so it is not visible and set external contrast so the brightness is 30FL. Switch to a display of cross hatch pattern.
2. Adjust the FBT focus VR1 and VR2 so the vertical line and horizontal line are as clear as possible.
3. Input a "o" characters pattern in primary mode and check "o" characters is clearest.

4.11. Color Misconvergence

1. Input a full white pattern in primary mode and adjust external brightness so there is no backguound brightness and external contrast so the screen brightness is 30FL.
2. Switch to a cross hatch pattern and verify that misconvergence in a circle measured from the center of the screen (Area A) is not greater than 0.3mm, and for all areas outside Area A is not greater than 0.4mm.

Automatic camera alignment procedure:

The procedures listed below are those carried out using the automatic Camera Alignment System (CAS). These adjustments cannot be made manually but must be performed using the CAS software provided by the manufacturer.

4.12. Primary Test Mode Performance Adjustments

1. V. RASTER CENTERING
   Raster area centered vertically in the bezel.
2. ROTATION (TILT)
   Raster area aligned with bezel.

4.13. Performance Adjustments for All Preset Modes

1. H POSITION
   Centers the picture display horizontally in the bezel area (L-R≤1mm).
2. H SIZE
   Configures picture display width as 300±3mm.
3. V POSITION
   Centers the picture display vertically in the bezel area (T-B≤1mm).

4. **V SIZE**
   Configures picture display height as 225±3mm.
5. **V Linearity**
   Configures vertical linearity as less than 8%.
6. **Rotation**
   Configures picture display rotation as less than 1mm.
7. **Pin-Balance**
   Sets left and right pin-balance distortion to less than 1.5mm.
8. **PINCUSHION**
   Sets left and right pincushion distortion to less than 1.5mm.
9. **Trapezium**
   Sets upper and lower trapezium distortion to less than 1.5mm.
10. **Parallelogram**
    Sets parallelogram distortion to less than 1.5mm.

Conclusion of automatic alignment:

4.14. Image Performance Verification

Input each of the preset timings and check that the following specifications are met:

1. **Horizontal Position**
   L-R≤3mm
2. **Horizontal Size**
   300±3mm
3. **Vertical Position**
   T-B≤3mm
4. **Vertical Size**
   225±3mm
5. **Horizontal Linearity**
   H≤10% (10 x 8 cross hatch pattern)
   This calculation is based on the following formula:

$$\frac{Max - Min}{Max} \times 100\% \leq 10\%$$

6. **Vertical Linearity**
   V≤8.0% (10x8 cross hatch pattern).

$$\frac{Max - Min}{Max} \times 100\% \leq 8\%$$

7. **Geometric Edge Distortion**
   All geometrics distortion shall be less than as below:
   Horizontal line ≤2.5mm
   Vertical line ≤2mm
8. **Recall Button Function**
   Adjust H/V phase and size at random using the external controls and press the recall button. Check that the image performance has returned to be in spec, which will indicate the recall button is functioning correctly.

4.15. Uniformity Verification

Input a 2" square pattern in primary mode, set contrast to maximum and check that there is no overshoot. Check that the brightness in the four corners of the screen is not less than 70% of that in the center of the screen.

4.16. Brightness Verification

1. Input a raster pattern (no video pattern) in primary mode. Adjust external brightness to 0.08FL.
2. Input a full white pattern and adjust external contrast to maximum then check that brightness at the center of the screen shall be more than 30FL. Adjust external brightness to maximum and check that brightness at the center of the screen is 39FL±3.

4.17. Display Size Stability

Inputer a full white pattern in primary mode, set external brightness at 5FL and measure the display size. Adjust the brightness to 30FL and remeasure the display size. The differeness should be less than 0.8mm.

4.18. Color Purity Verification

1. Input a full white pattern in primary mode and adjust external brightness so there is no background brightness and adjust external contrast to 25FL. Make a visual check of color purity as follows:

   a)Input the red (R) signal only; no green (G) or blue (B) should be visible.

   b)Input the G signal only; no R or B should be visible.

   c)Input the B signal only; no R or G should be visible.

4.19. Video Noise

Input a cross hatch pattern or full white pattern in primary mode and make a visual check from a distance of 48.3cm (19 inches) for any video noise or other on-screen interference.

4.20. Power Saving Check

1. Input cross hatch pattern in primary mode.
2. Turn OFF H-Sync signal, the power indicator LED have to change the emitting color from green to orange, then turn ON H-Sync signal again, the picture shall be visible.
3. Turn OFF V-Sync signal, the power indicator LED have to change the emitting color from green to orange, then turn ON V-Sync signal again, the picture shall be visible.
4. Turn OFF H/V-Sync signal, the power indicator LED have to change the emitting color from green to orange, then turn ON H/V-Sync signal again, the picture shall be visible.

4.21. Audio Power Amplifier Check

Input audio signal from the audio signal generator to U.U.T of the audio in R/L side. Make a visual check of audio amplifier as follows:

1. Push L-side switch on fixture and check the U.U.T of the L-side speaker out.
2. Push R-side switch on fixture and check the U.U.T of the R-side speaker out.
3. Push L/R-side switch on fixture and check the U.U.T of the L/R-side speaker out.
4. Push phone switch on fixture and check the U.U.T of the phone jack out.

4.22. DDC 1/2 Data Writing

Writing the DDC 1/2 data in EEROM.

Section 5.
Troubleshooting

5.1. No Display at Power-on 5-1
5.2. No X-ray Operation 5-2
5.3. No Video Operation 5-3
5.4. Poor Vertical Linearity 5-4
5.5. Poor Horizontal Linearity 5-5
5.6. Poor Uniformity 5-6
5.7. Tilted Display Area 5-7
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5.9. Poor Regulation 5-9
5.10. Poor Focus 5-10
5.11. Poor Geometry 5-11
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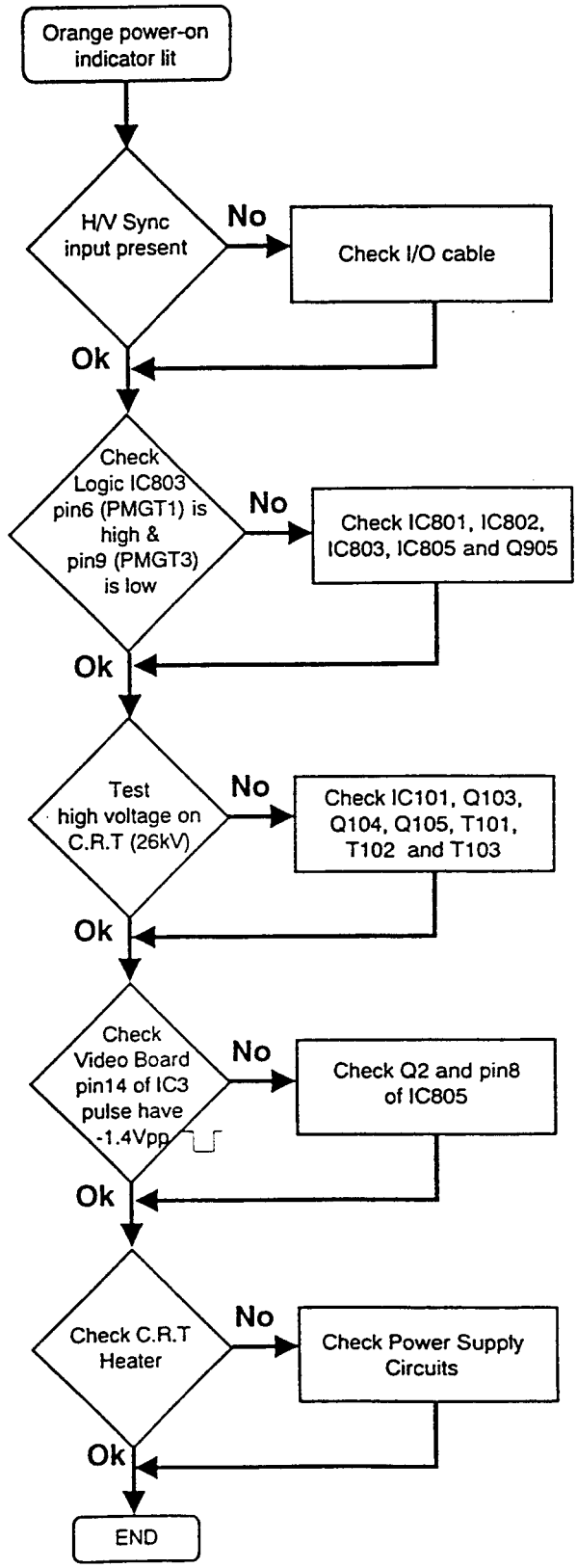
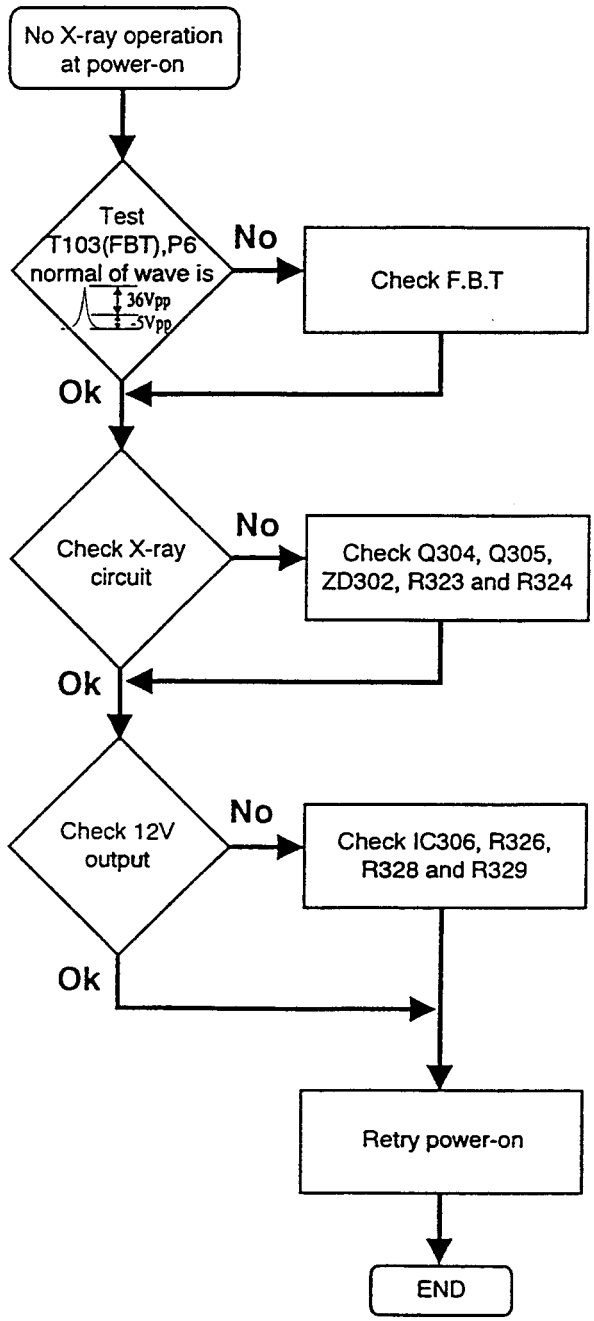
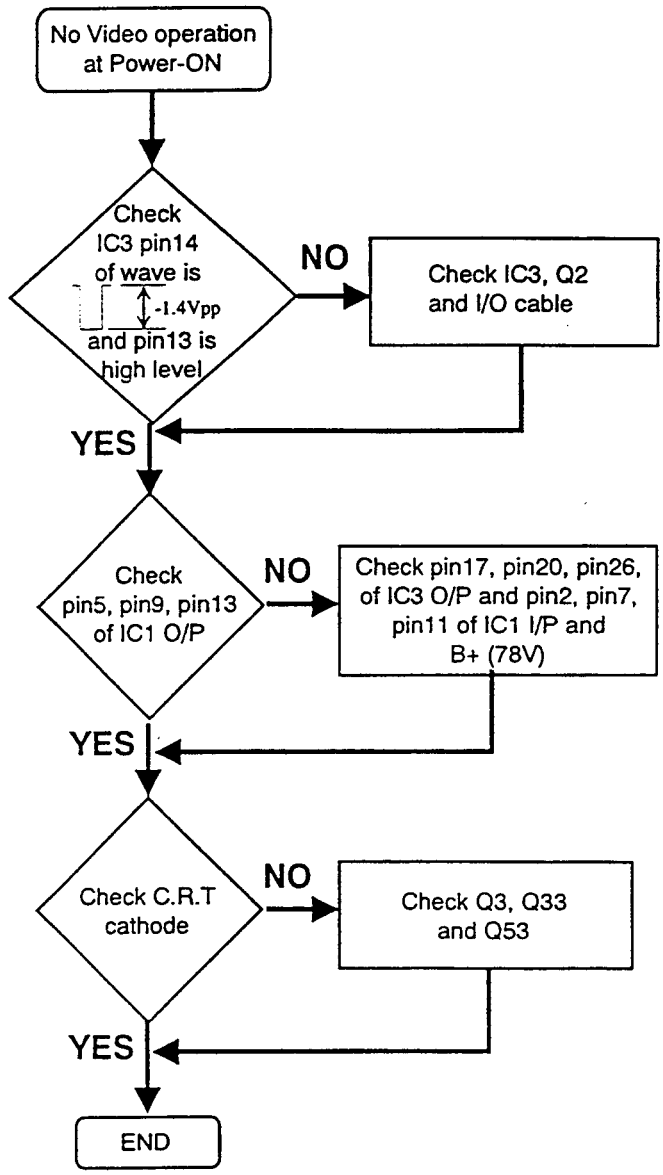
5.1. No Display at Power-on



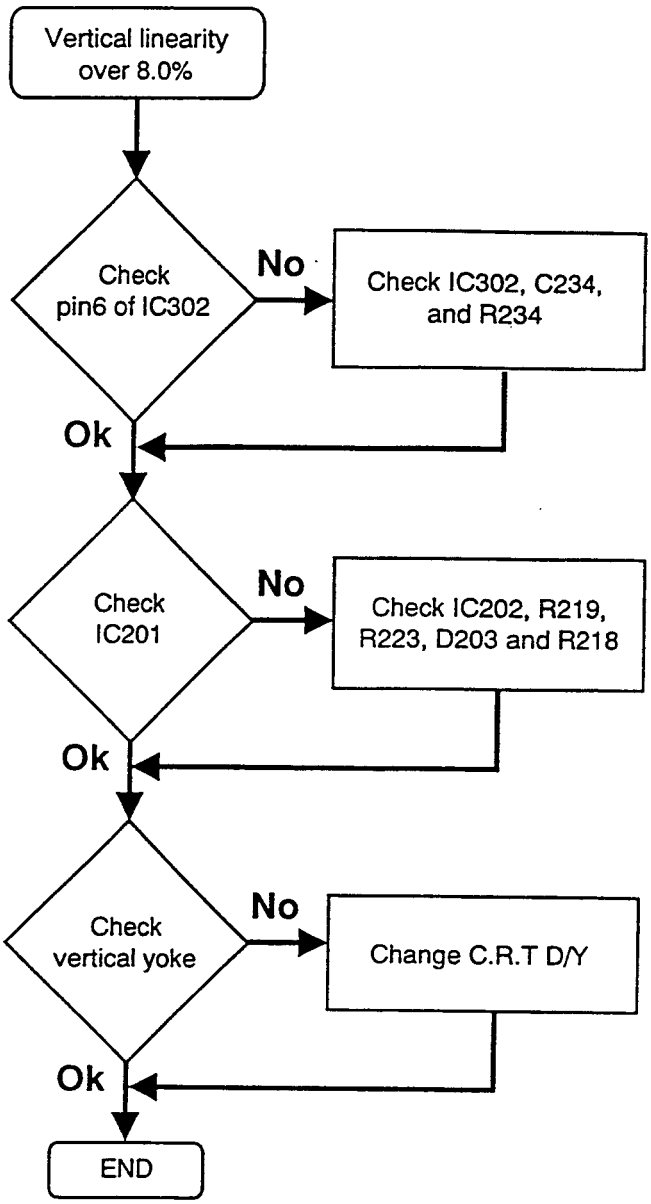
5.2. No X-ray Operation



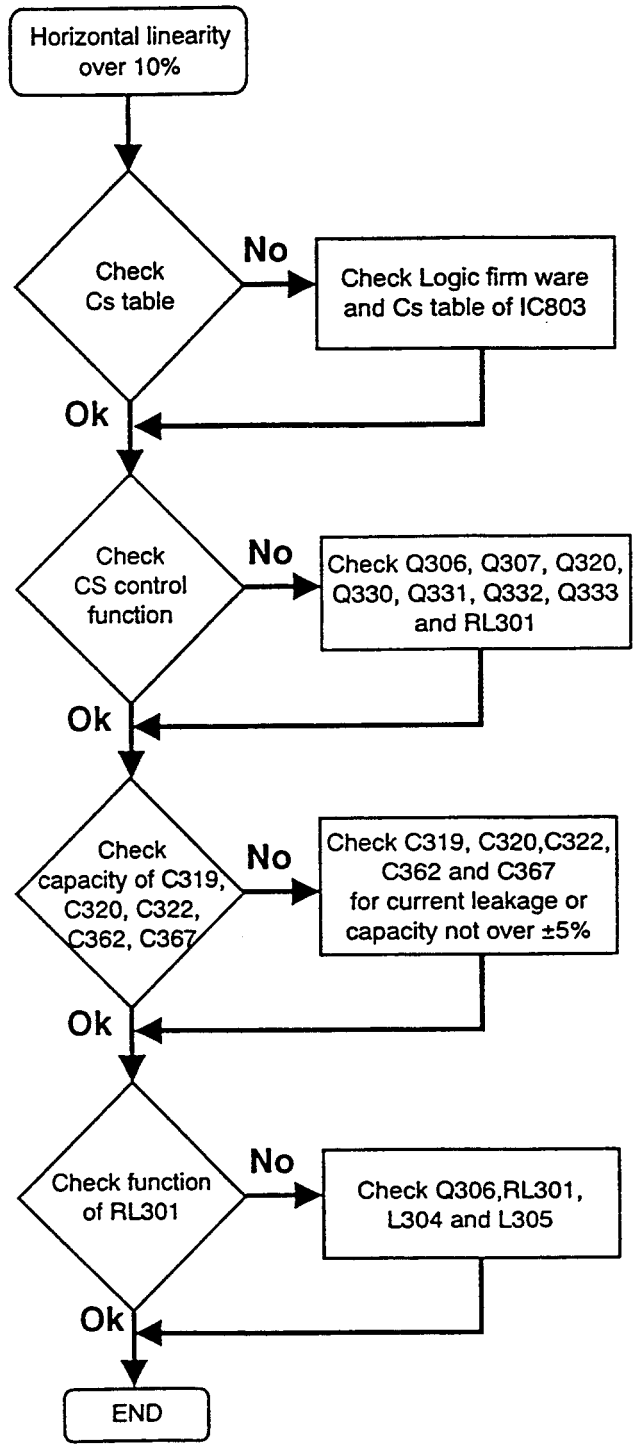
5.3. No Video Operation



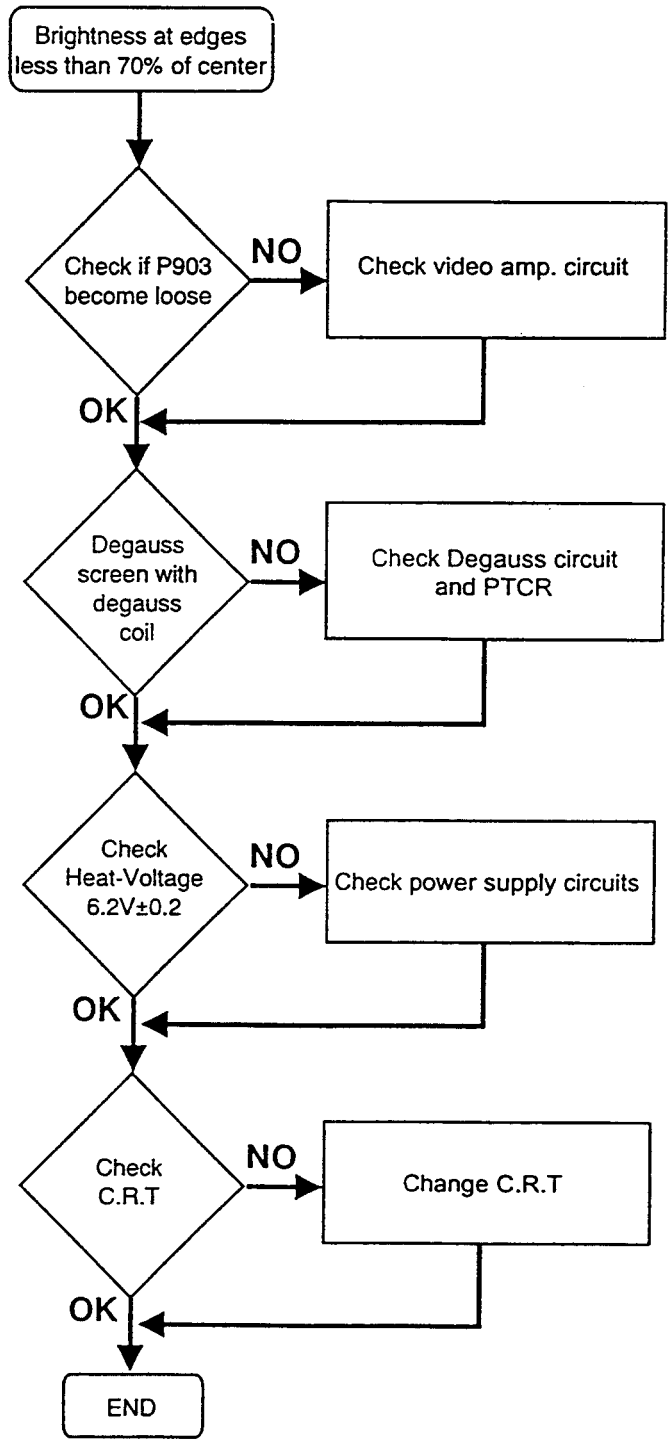
5.4. Poor Vertical Linearity



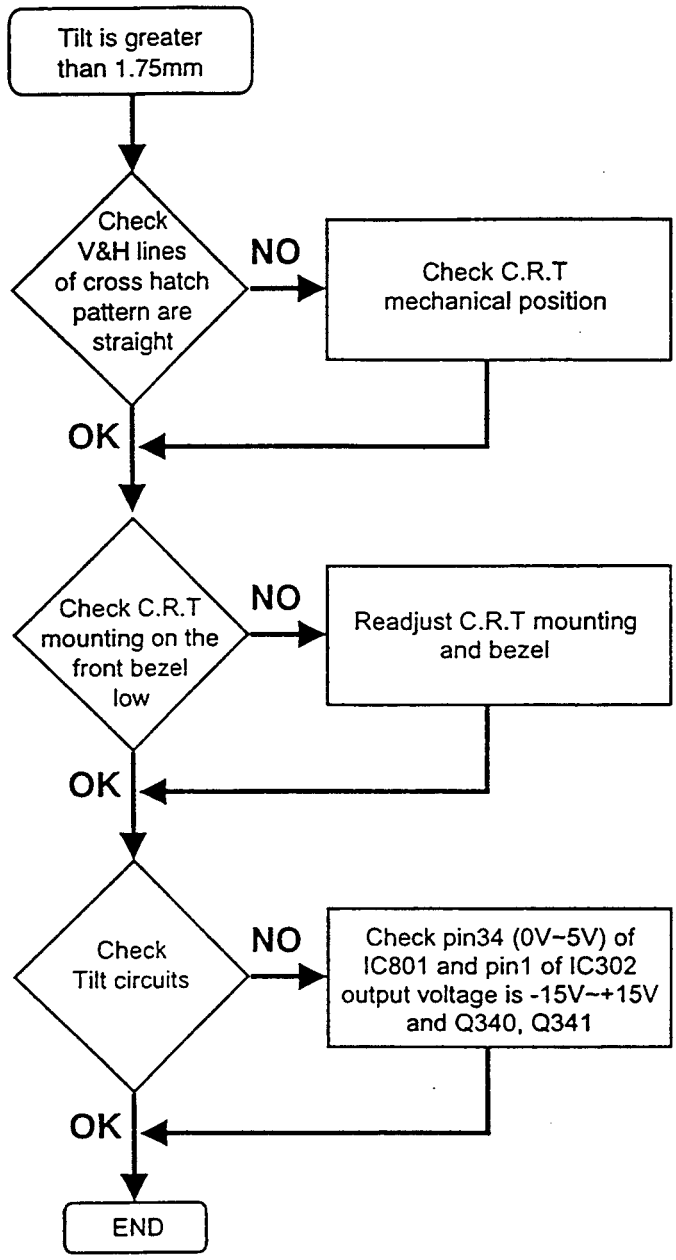
5.5. Poor Horizontal Linearity



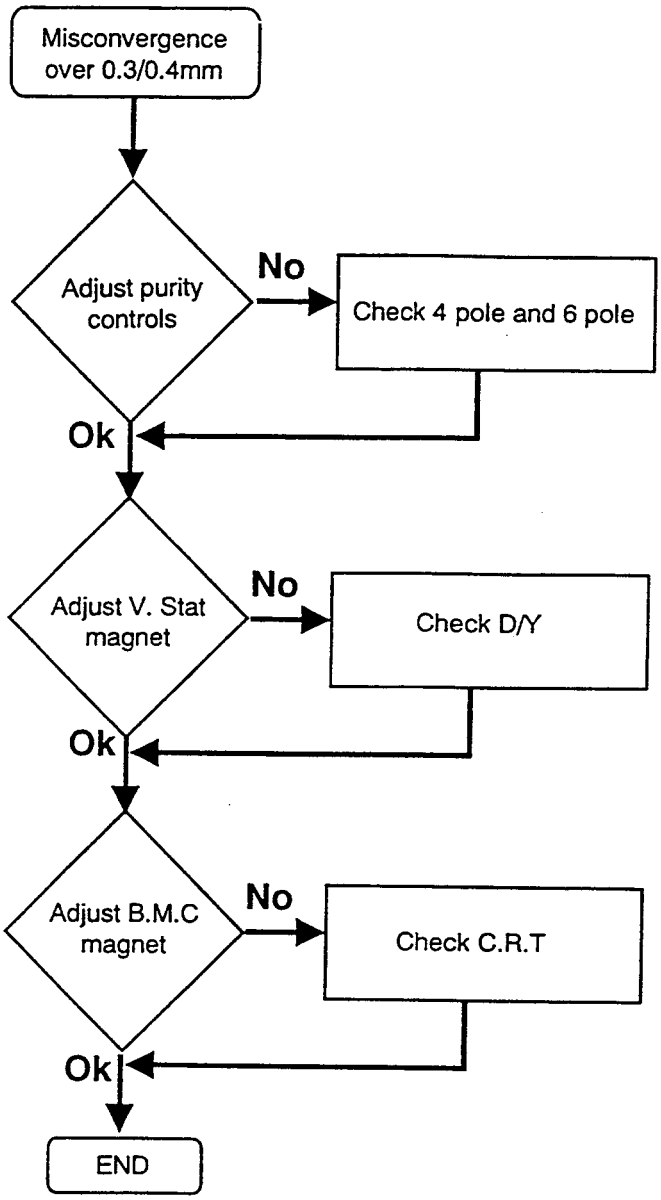
5.6. Poor Uniformity



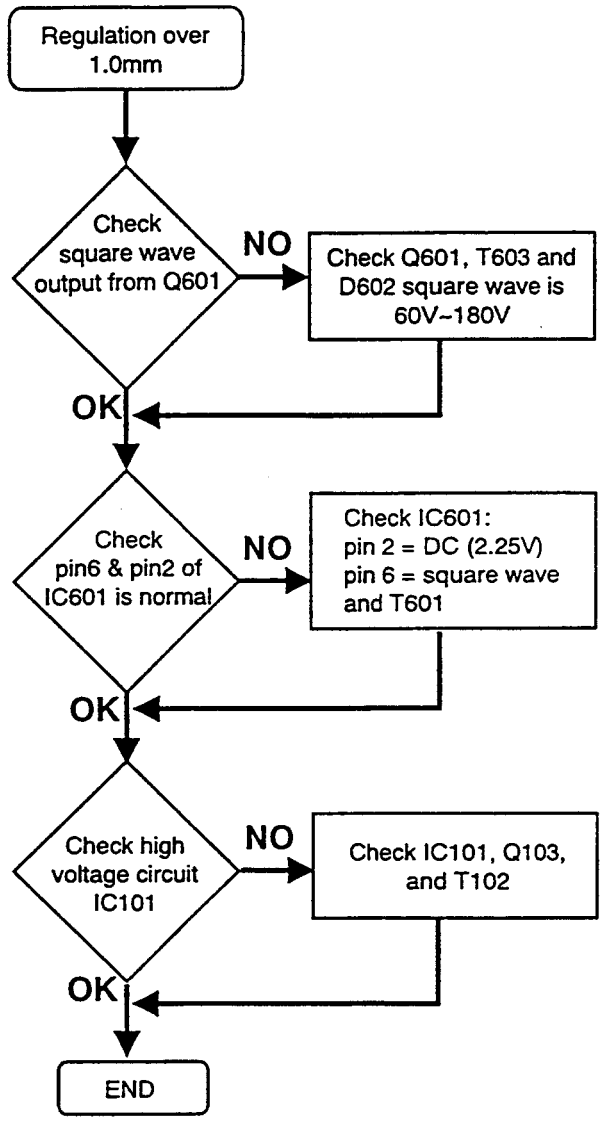
5.7. Tilted Display Area


Tilt is greater than 1.75mm
Check V&H lines of cross hatch pattern are straight
NO
Check C.R.T mechanical position
OK
Check C.R.T mounting on the front bezel low
NO
Readjust C.R.T mounting and bezel
OK
Check Tilt circuits
NO
Check pin34 (0V~5V) of IC801 and pin1 of IC302 output voltage is -15V~+15V and Q340, Q341
OK
END

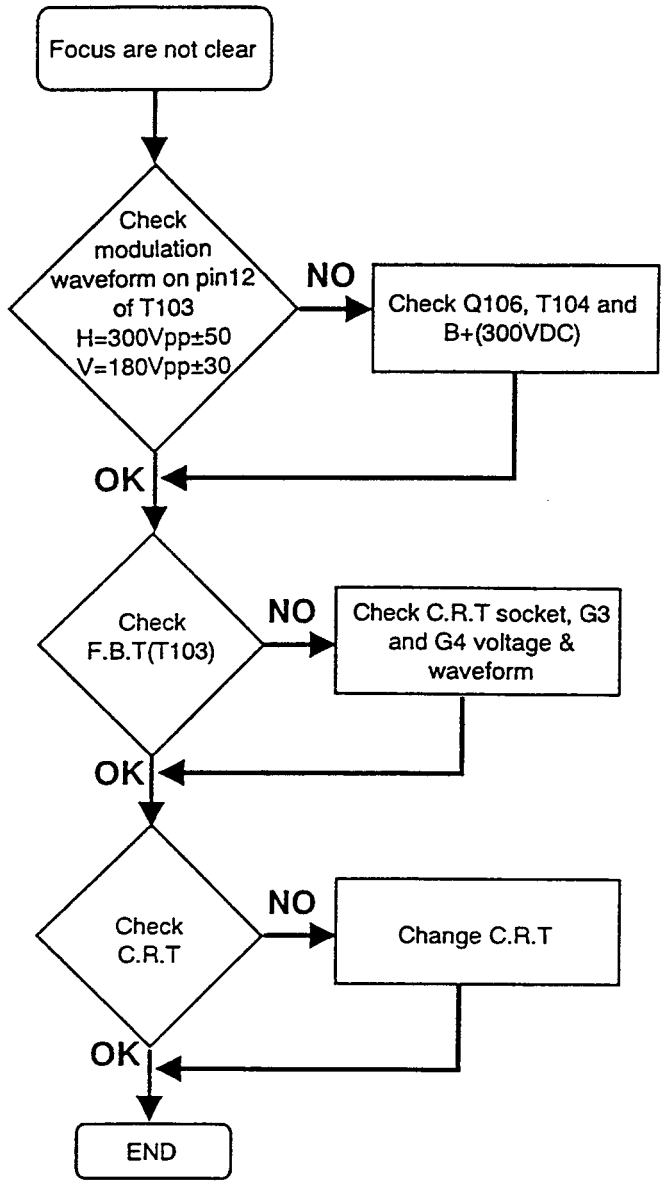
5.8. Misconvergence



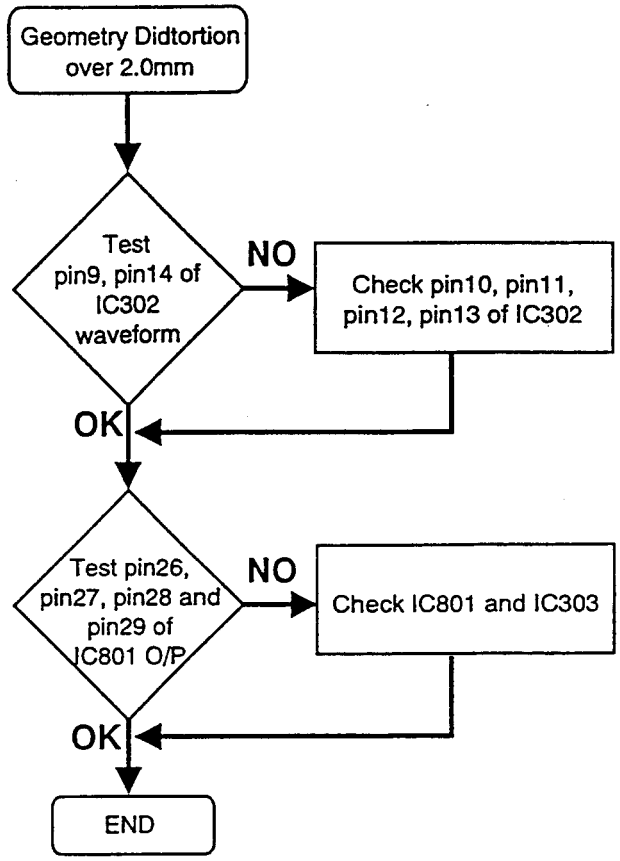
5.9. Poor Regulation


Regulation over 1.0mm
Check square wave output from Q601
NO
Check Q601, T603 and D602 square wave is 60V~180V
OK
Check pin6 & pin2 of IC601 is normal
NO
Check IC601: pin 2 = DC (2.25V) pin 6 = square wave and T601
OK
Check high voltage circuit IC101
NO
Check IC101, Q103, and T102
OK
END

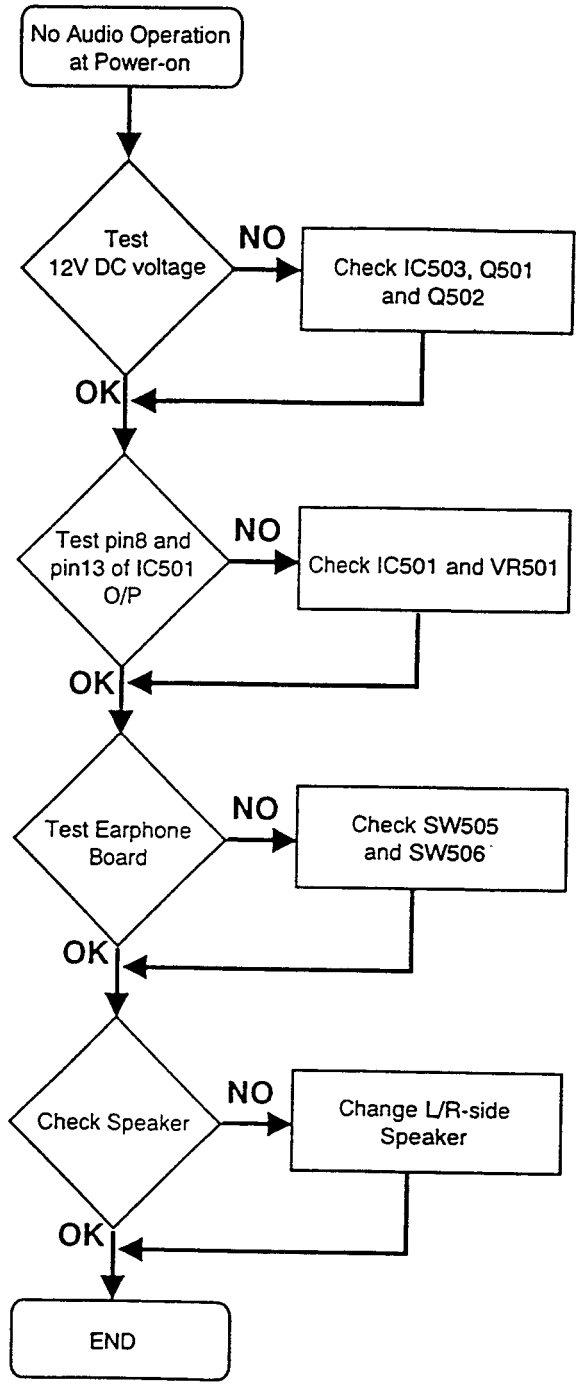
5.10. Poor Focus



5.11. Poor Geometry Distortion



5.12. No Audio Amplifier



Notes

Section 6.
Printed Circuit Boards

6.1. Neck Board 6-1
6.2. Main Board 6-2
6.3. Control Board 6-3
6.4. Earphone Board 6-3
6.5. PCB Wiring Connection 6-4

6.1. Neck Board

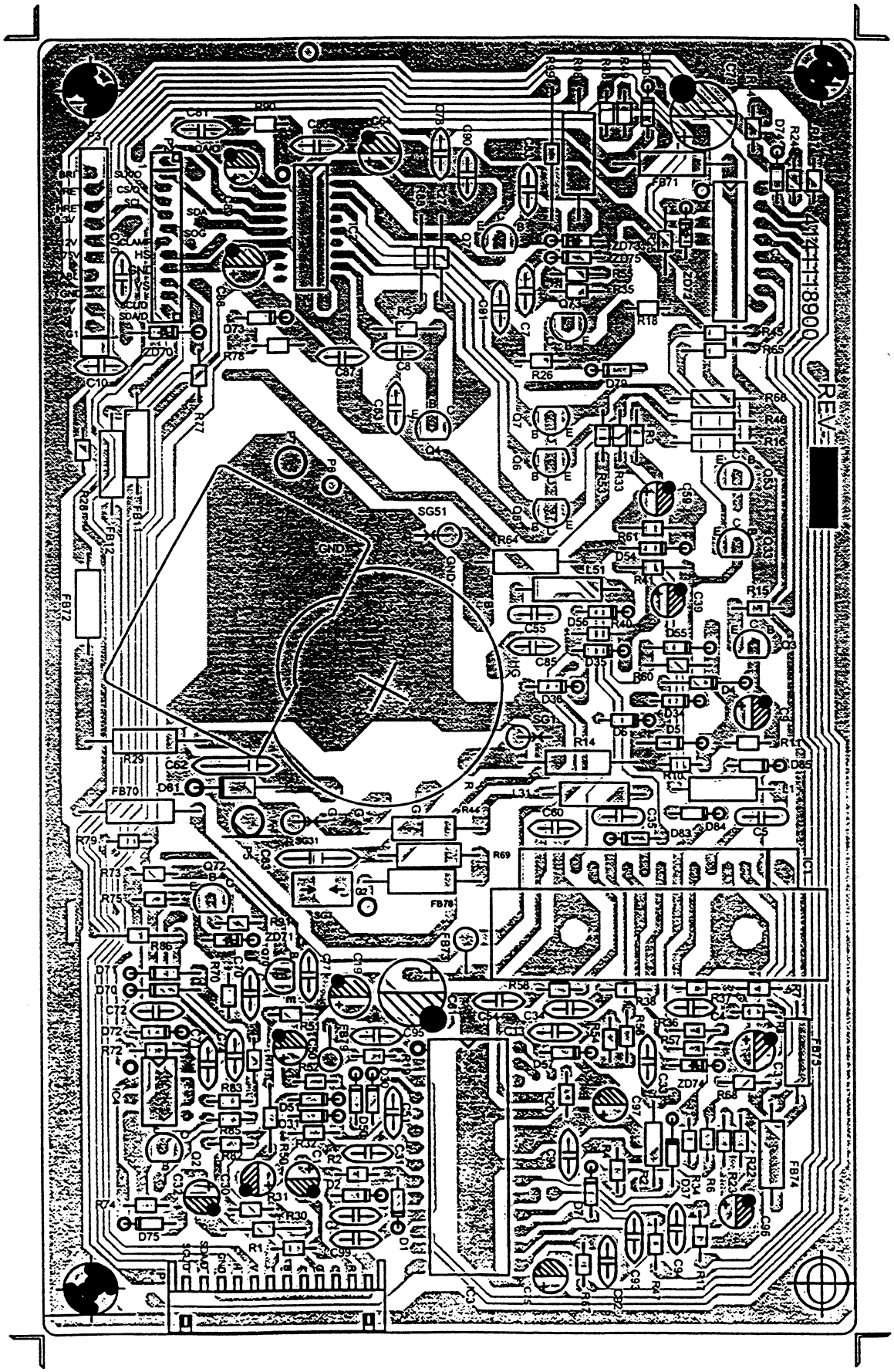


Figure 6-1 Neck Board (Solder Side)

6.2. Main Board

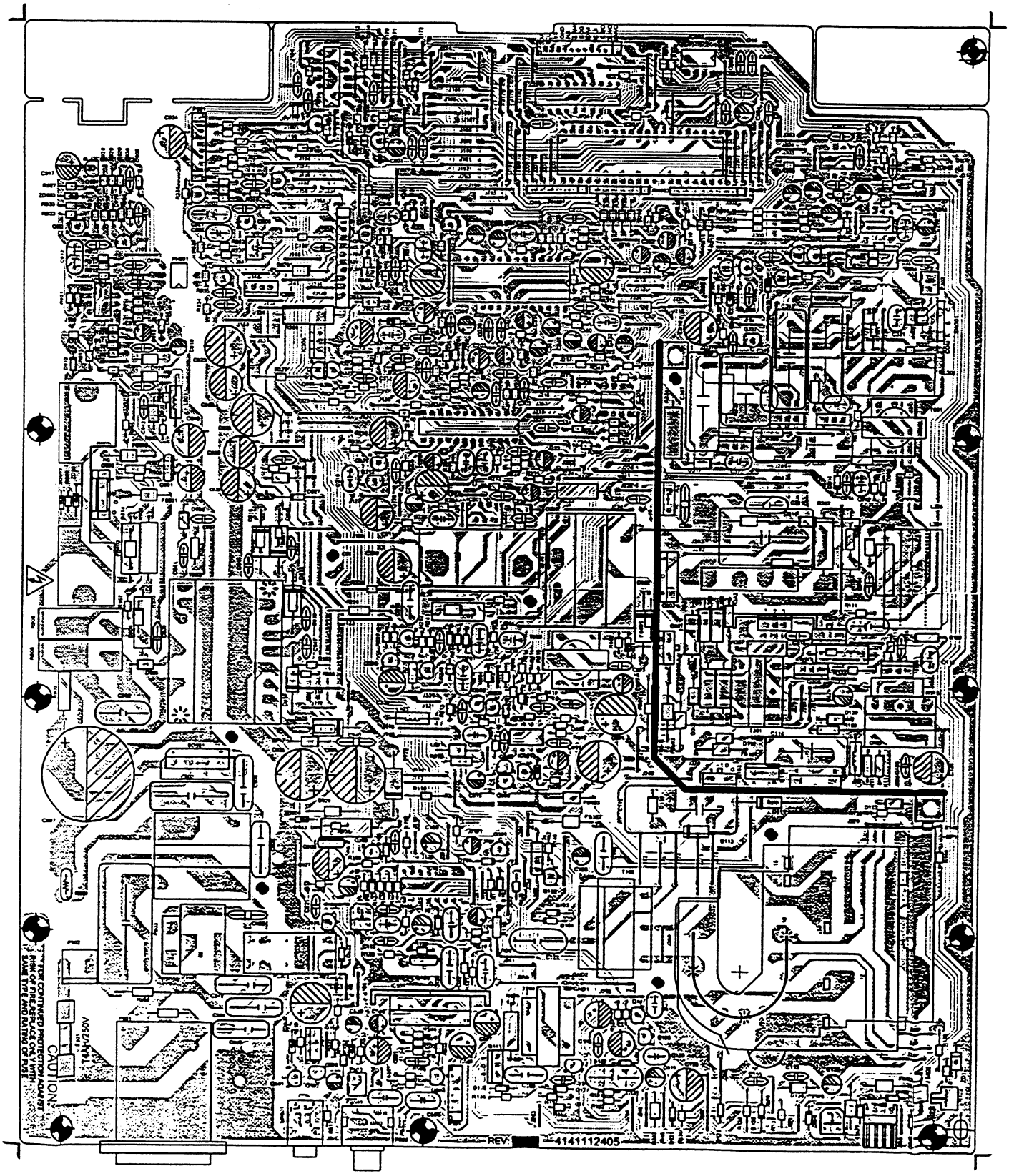


Figure 6-2 Main Board (Solder Side)

6.3. Control Board

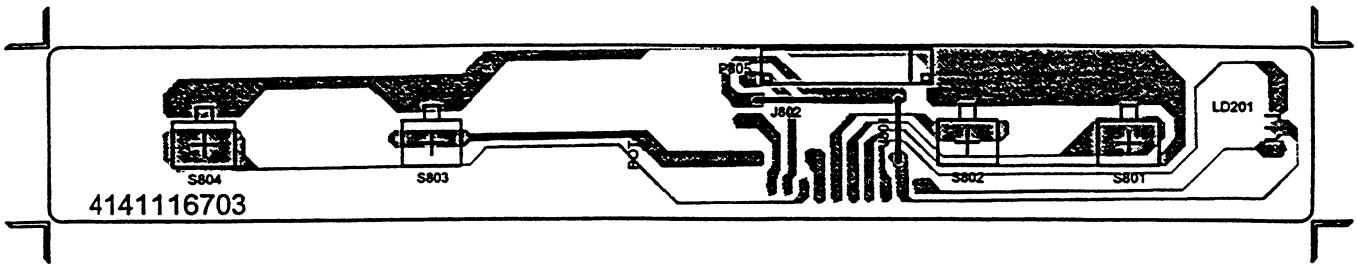


Figure 6-3 Control Board (Solder Side)

6.4. Earphone Board

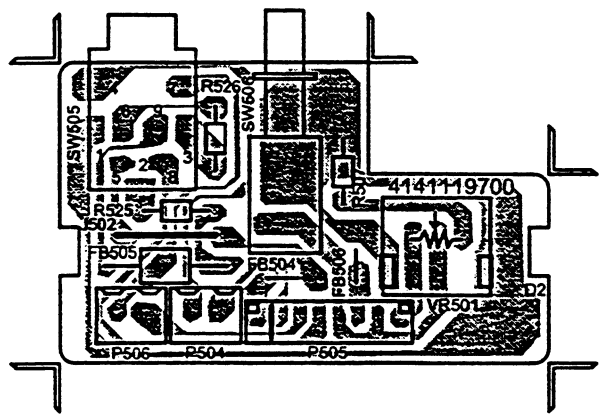


Figure 6-4 Earphone Board (Solder Size)

6.5. PCB Wiring Connection

1. Original model:

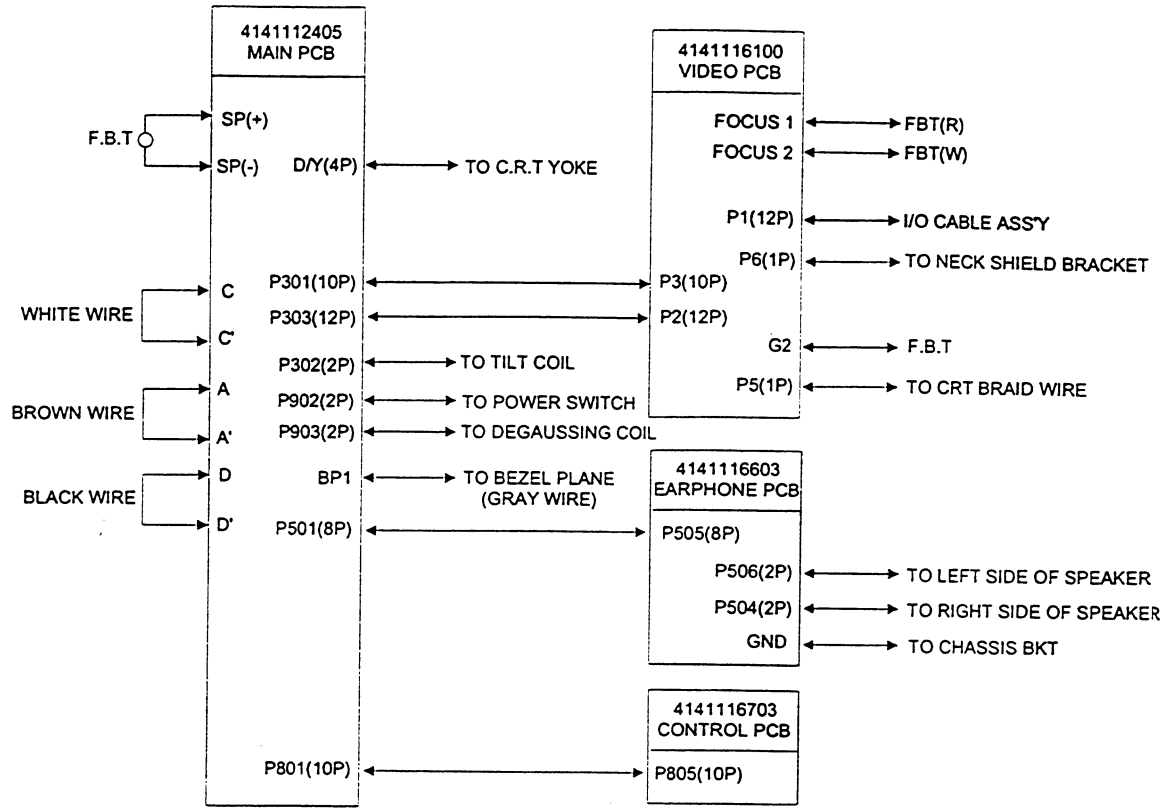


Figure 6-6 PCB Wiring Connection (original)

2. Current model:

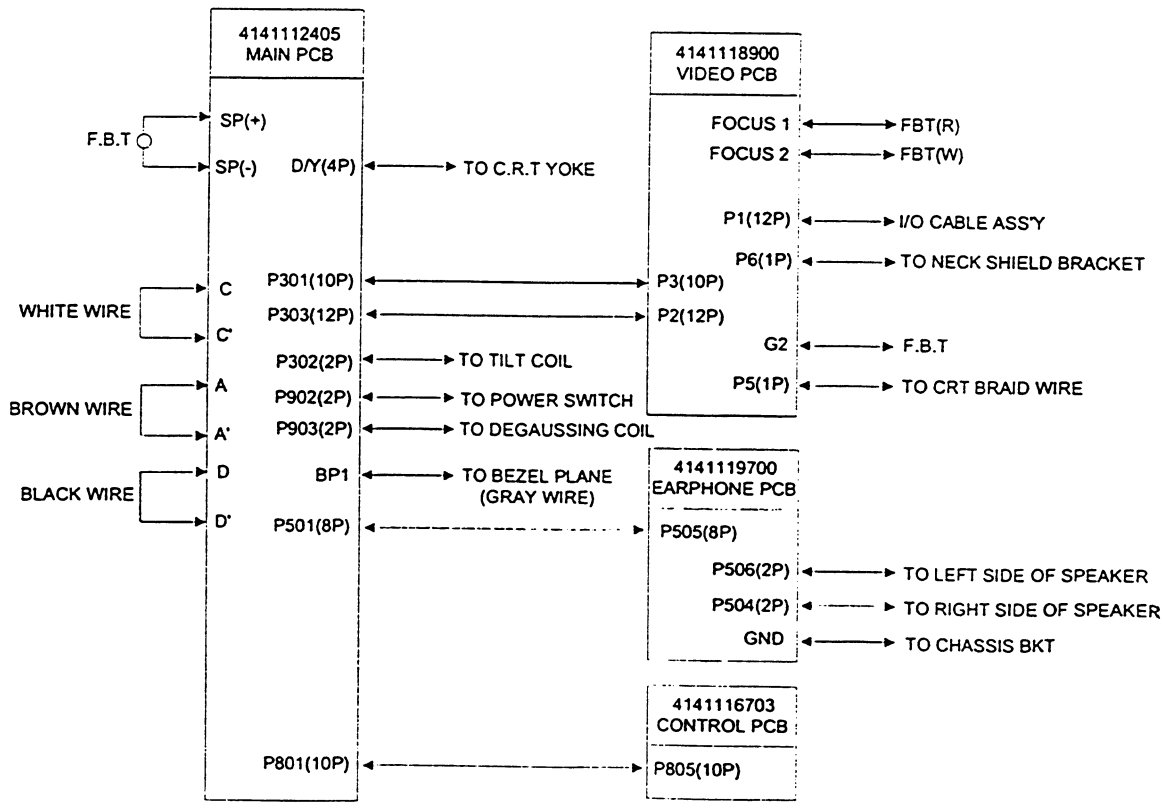


Figure 6-5 PCB Wiring Connection (current)

Notes

Section 7.
Schematic Diagrams

7.1. Video Circuit Diagram 7-1
7.2. Deflection & S/P/S & Logic Circuit Diagram 7-1

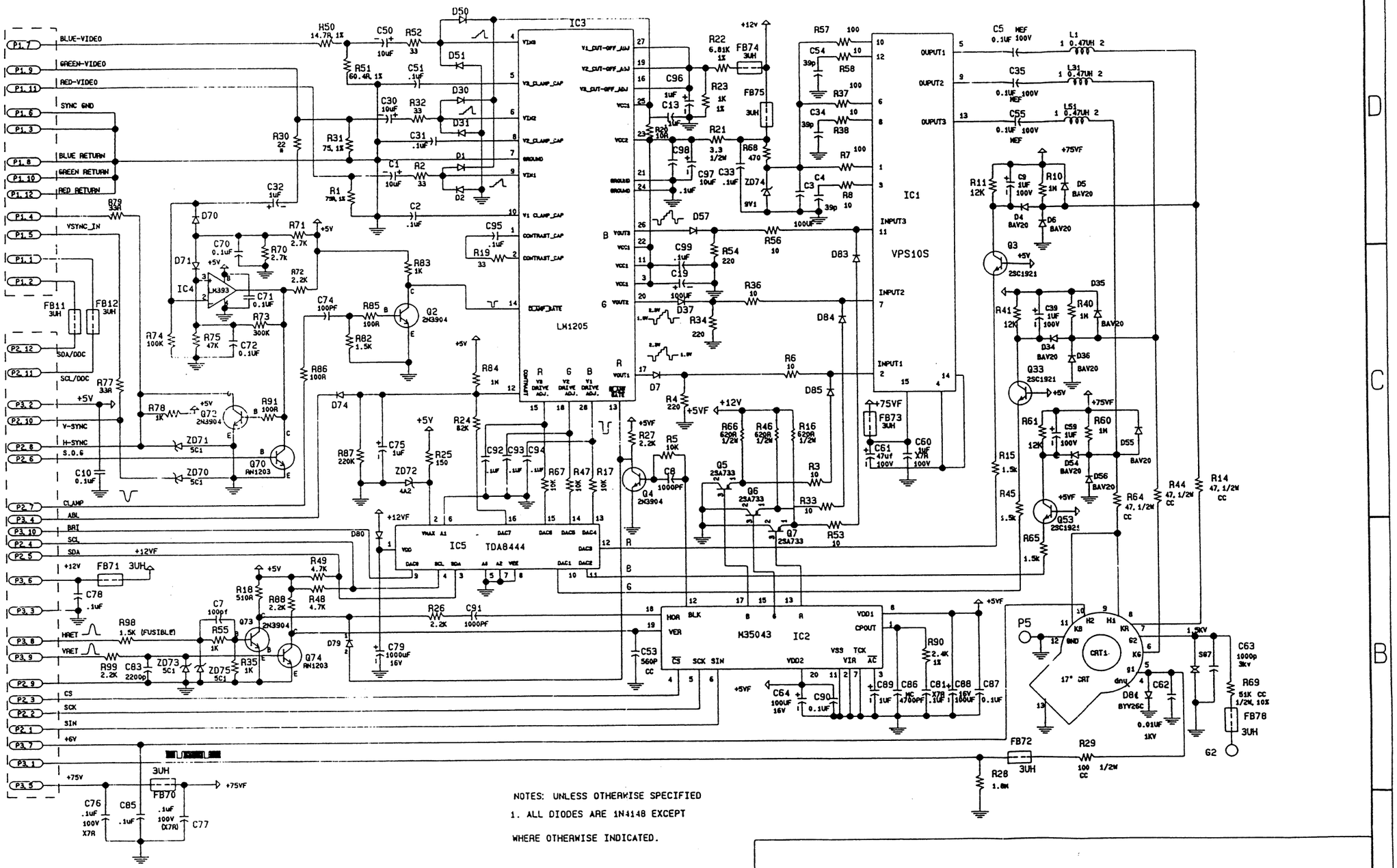
7.1. Video Circuit Diagram

Please refer to the attached circuit diagram.

7.2. Deflection & S/P/S & Logic Circuit Diagram

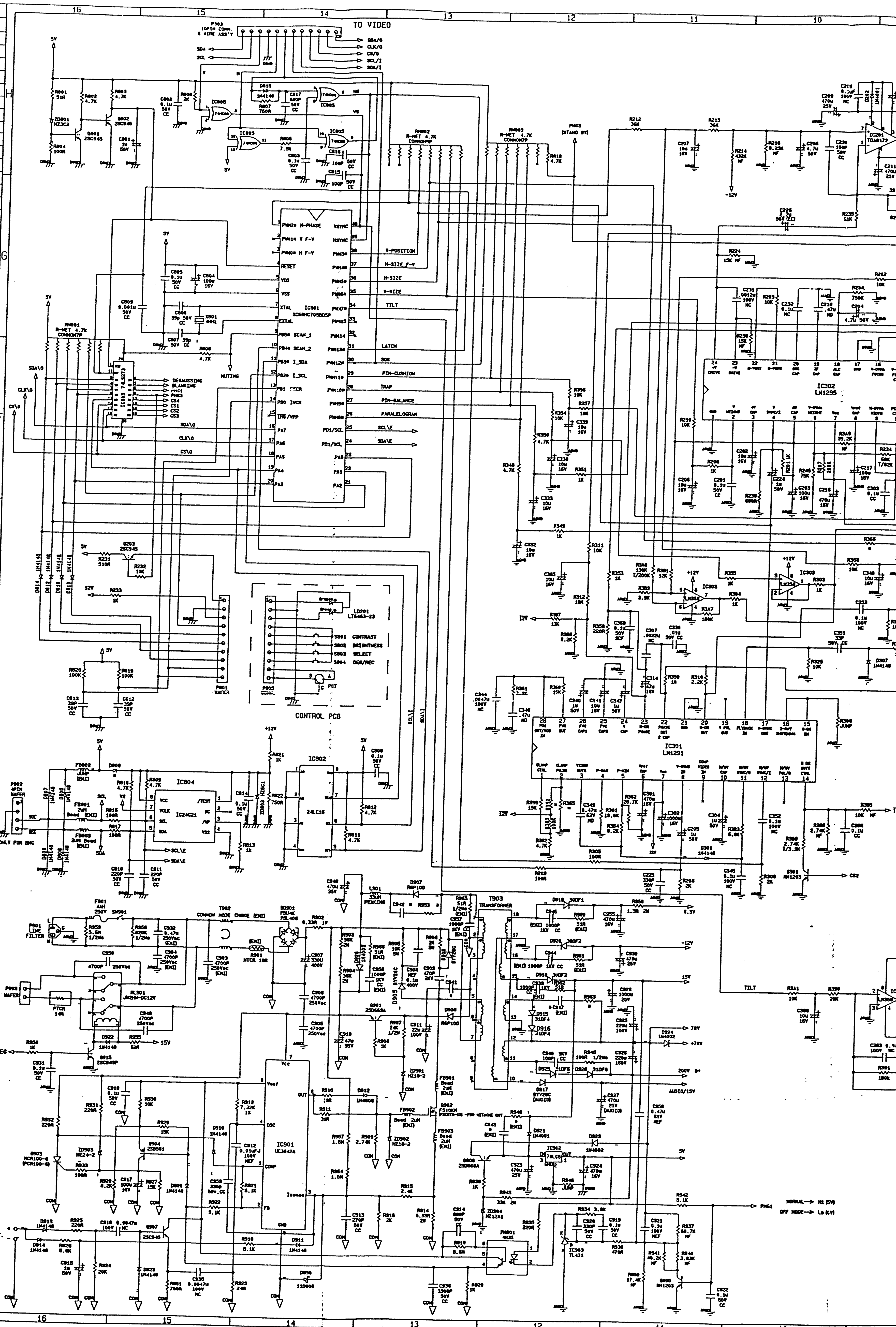
Please refer to the attached circuit diagram.

DATE	ECN/ECO NO.
08-12-'96	0-08029602ET
10-23-'96	0-091696C1AT

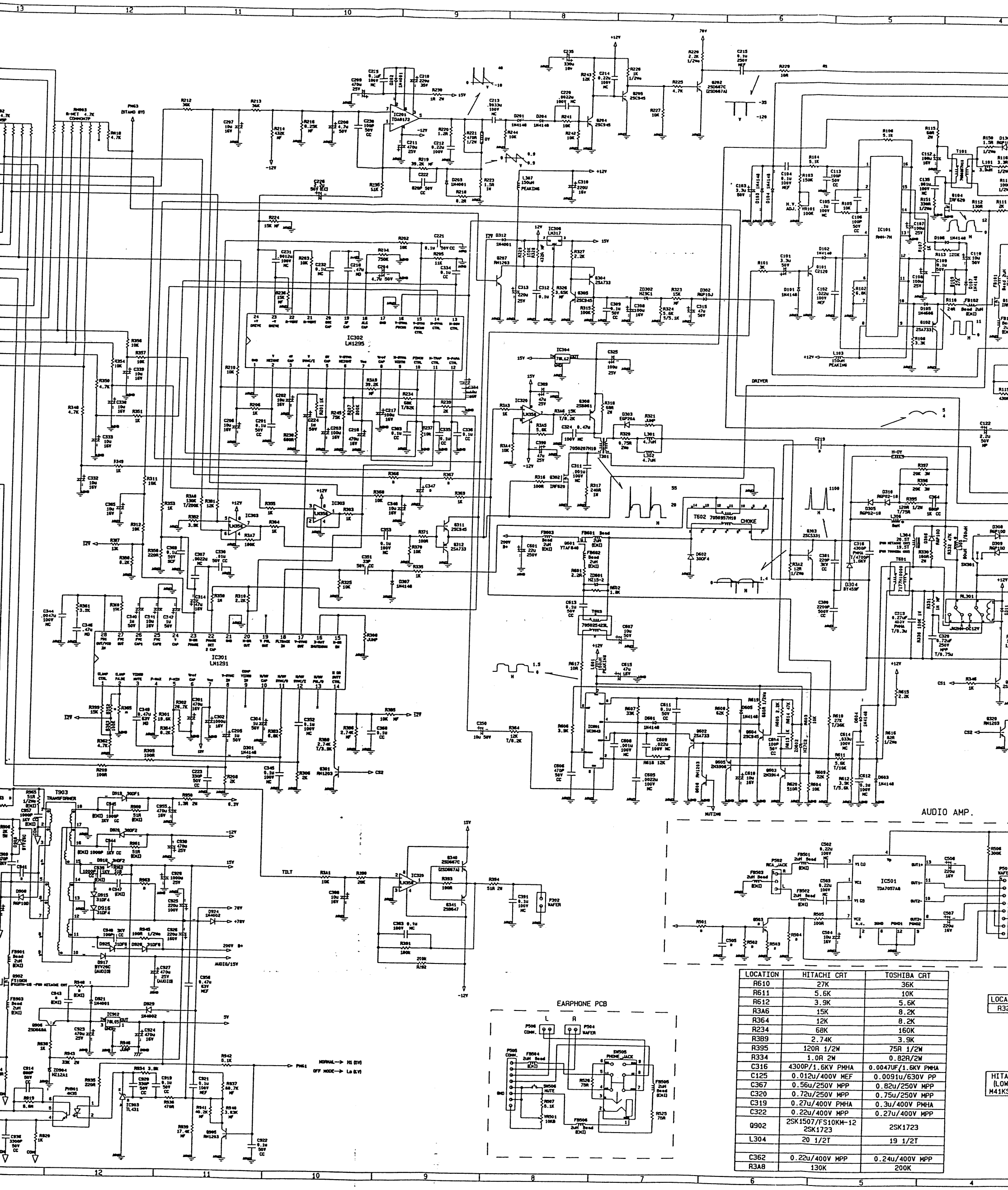


DRAWING DATE	TOLERANCE		SCALE	UNIT
10-23-'96	DIM	ANGLE	/	MM
	+ -	+ -		
DRAWER	SHEET		DRAWING NAME	FILENAME
LIN	1 OF 1		VIDEO	RH7HXX2A
MODEL NO: RMH-7HXX.RMS-7KXX.RTS-7K2X.RTH-7H2X				

DATE	ECN/ECO NO.
03-14-'96	C—[illegible]129601ET
03-15-'96	C—[illegible]149603ET
03-26-'96	C—[illegible]019601ET
03-28-'96	C—[illegible]259609ET
03-28-'96	C—[illegible]259608ET
04-11-'96	C—[illegible]029601ET
04-11-'96	C—[illegible]199607ET
04-11-'96	C—[illegible]089603ET
04-26-'96	N—[illegible]109601EG
05-15-'96	C—[illegible]039603RC
05-29-'96	C—[illegible]039604RC
05-31-'96	C—[illegible]079601RP
09-24-'96	C—[illegible]2796C4ET
10-02-'96	C—[illegible]239602RP



TO VIDEO
P303 10PIN CONN. 8 WIRE ASS'Y
IC801 XC68HC705BD5P
IC803 74LS273
DEGAUSSING
BLANKING
MUTING
V-POSITION
H-SIZE F-V
H-SIZE
V-SIZE
TILT
LATCH
SOG
PIN-CUSHION
TRAP
PIN-BALANCE
PARALELOGRAM
LD201 LT6463-23
S801 CONTRAST
S802 BRIGHTNESS
S803 SELECT
S804 DEG/REC
POT
CONTROL PCB
IC804 IC24C21
IC802 24LC16
ONLY FOR BNC
IC302 LM1295
IC201 TDA8172
IC301 LM1291
IC303 LM358
P901 LINE FILTER
F901 4AH 250V
SW901
T902 COMMON MODE CHOKE (EMI)
BD901 FBU4K PBL406
RL901 JM2HN-DC12V
PTCR 14M
T903 TRANSFORMER
L901 33uH PEAKING
IC901 UC3842A
IC902 78L05
IC903 TL431
PH901 4N35
FROM F.B.T.
6.3V
-12V
15V
78V
+78V
200V B+
AUDIO/15V
5V
PM61
NORMAL—> Hi (5V)
OFF MODE—> Lo (0V)



LOCATION	HITACHI CRT	TOSHIBA CRT
R610	27K	36K
R611	5.6K	10K
R612	3.9K	5.6K
R3A6	15K	8.2K
R364	12K	8.2K
R234	68K	160K
R389	2.74K	3.9K
R395	120R 1/2W	75R 1/2W
R334	1.0R 2W	0.82R/2W
C316	4300P/1.6KV PMHA	0.0047UF/1.6KV PMHA
C125	0.012u/400V MEF	0.0091u/630V PP
C367	0.56u/250V MPP	0.82u/250V MPP
C320	0.72u/250V MPP	0.75u/250V MPP
C319	0.27u/400V PMHA	0.3u/400V PMHA
C322	0.22u/400V MPP	0.27u/400V MPP
Q902	2SK1507/FS10KM-12 2SK1723	2SK1723
L304	20 1/2T	19 1/2T
C362	0.22u/400V MPP	0.24u/400V MPP
R3A8	130K	200K

	30K-34K	34K-39K	39K-45K	45K-55K	55K-69.5K	69.5K-85K
CS1	L	L	L	H	H	H
CS2	L	L	L	L	H	H
CS3	L	L	H	L	L	H
CS4	L	H	H	H	H	H

AUDIO AMP.

MICROPHONE

EARPHONE PCB

LOCATION	HITACHI CRT	TOSHIBA CRT
R610	27K	36K
R611	5.6K	10K
R612	3.9K	5.6K
R3A6	15K	8.2K
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R3B9	2.74K	3.9K
R395	120R 1/2W	75R 1/2W
R334	1.0R 2W	0.82R/2W
C316	4300P/1.6KV PMHA	0.0047UF/1.6KV PMHA
C125	0.012u/400V MEF	0.0091u/630V PP
C367	0.56u/250V MPP	0.82u/250V MPP
C320	0.72u/250V MPP	0.75u/250V MPP
C319	0.27u/400V PMHA	0.3u/400V PMHA
C322	0.22u/400V MPP	0.27u/400V MPP
Q902	2SK1507/FS10KM-12 2SK1723	2SK1723
L304	20 1/2T	19 1/2T
C362	0.22u/400V MPP	0.24u/400V MPP
R3A8	130K	200K

LOCATION	MATSUSHITA FBT	SAMPO FBT
R324	5.6K	5.1K

HITACHI CRT (LOW POWER) M41KSX180X11	R950
	3R 2W

NOTE: * 7HXX WITHOUT AUDIO, EARPHONE & MIC.
* 7KXX WITH AUDIO & EARPHONE.
* ONLY 7K21 WITH AUDIO, EARPHONE & MIC.

10 55 96

DRAWING DATE	TOLERANCE		SCALE	UNIT
11-01-96	DIM + -	ANGLE + -	/	MM
DRAWER	SHEET		DRAWING NAME	FILENAME
LO	1 OF 1		DEF & SPS & LOGIC	RH7HXX1A
MODEL NO:	RMH-7HXX.RMS-7KXX.RTS-7K2X.RTH-7H2X			